



24-BIT, 96/192-KHZ ASYNCHRONOUS STEREO AUDIO CODEC

FEATURES

- 24-Bit Delta-Sigma ADC and DAC
- ADC, DAC Asynchronous Operation
- Stereo ADC:
 - High Performance: (Typical, 48 kHz)
 - THD+N: –93 dB
 - SNR: 99 dB
 - Dynamic Range: 99 dB
 - Sampling Rate: 16–96 kHz
 - System Clock: 256, 384, 512, 768 f_s
 - Full Scale Input: 3 V_{p-p}
 - Antialiasing Filter Included
 - 1/64 Decimation Filter:
 - Pass-Band Ripple: ± 0.05 dB
 - Stop-Band Attenuation: –65 dB
 - On-Chip High-Pass Filter: 0.91 Hz at $f_s = 48$ kHz
- Stereo DAC:
 - High Performance: (Typical, Differential, 48 kHz)
 - THD+N: –94 dB
 - SNR: 105 dB
 - Dynamic Range: 104 dB
 - Sampling Rate: 16–192 kHz
 - System Clock: 128, 192, 256, 384, 512, 768 f_s
 - Differential Voltage Output: 8 V_{p-p}
 - Single-Ended Voltage Output: 4 V_{p-p}
 - Analog Low-Pass Filter Included
 - 4 \times /8 \times Oversampling Digital Filter:
 - Pass-Band Ripple: ± 0.04 dB
 - Stop-Band Attenuation: –50 dB
 - Zero Flags
- Flexible Mode Control
 - 3-Wire SPI, 2-Wire I²C Compatible Serial Control Interface
 - Hardware Control Mode
- Multiple Functions via SPI or I²C Interface:
 - Digital Attenuation and Soft Mute for ADC

and DAC

- Digital De-Emphasis: 32, 44.1, 48 kHz for DAC
- Power Down: ADC/DAC Independently
- Asynchronous/Synchronous Control for ADC/DAC Operation
- External Reset and Power-Down Pin:
 - ADC/DAC Simultaneously
- Audio Interface Mode:
 - ADC/DAC Independent Master/Slave
- Audio Data Format:
 - ADC/DAC Independent
 - I²S, Left-Justified, Right-Justified
- Dual Power Supplies:
 - 5-V for Analog and 3.3-V for Digital
- Package: TSSOP-28

APPLICATIONS

- DVD-RW
- Digital TV
- Digital Set-Top Box
- Audio-Visual Applications

DESCRIPTION

The PCM3060 is a low-cost, high-performance, single-chip, 24-bit stereo audio codec with single-ended analog inputs and differential analog outputs.

The stereo 24-bit ADC employs a 64-times delta-sigma modulator. It supports 16–96 kHz sampling rates and a 16/24-bit digital audio output word on the audio interface.

The stereo 24-bit DAC employs a 64- or 128-times delta-sigma modulator. It supports 16–192 kHz sampling rates and a 16/24-bit digital audio input word on the audio interface.

The PCM3060 supports fully independent operation of the sampling rate and audio interface for the ADC and DAC.

Each audio interface supports I²S, left-justified, and right-justified formats with 16/24-bit words.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The PCM3060 can be software-controlled through a 3-wire SPI-compatible or 2-wire I²C-compatible serial interface, which provides access to all functions including digital attenuation, soft mute, de-emphasis etc.

The PCM3060 can be also used in hardware mode, which provides three basic functions.

The PCM3060 is fabricated using a highly advanced CMOS process and is available in a small 28-pin TSSOP package.

The PCM3060 is suitable for various sound processing applications for DVD-RW, digital TV, STB, and other AV equipment.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | VALUE | UNIT |
|--|--|---|------|
| Supply voltage | V _{CC} | -0.3 to 6.5 | V |
| | V _{DD} | -0.3 to 4 | |
| Ground voltage differences | AGND1, AGND2, DGND, SGND | ±0.1 | V |
| Digital input voltage | RST, MS, MC, MD, SCKI1, SCKI2, DIN | -0.3 to 6.5 | V |
| | BCK1, BCK2, LRCK1, LRCK2, DOUT | -0.3 to (V _{DD} + 0.3 V) < 4 | V |
| | ZEROL, ZEROR, MODE | -0.3 to (V _{DD} + 0.3 V) < 4 | V |
| Analog input voltage | V _{INL} , V _{INR} , V _{COM} , V _{OUTL+} , V _{OUTL-} , V _{OUTR+} , V _{OUTR-} | -0.3 to (V _{CC} + 0.3 V) < 6.5 | V |
| Input current (any pins except supplies) | | ±10 | mA |
| T _A | Ambient temperature under bias | -40 to 125 | °C |
| T _{stg} | Storage temperature | -55 to 150 | °C |
| T _J | Junction temperature | 150 | °C |
| Lead temperature (soldering) | | 260, 5 s | °C |
| Package temperature (IR reflow, peak) | | 260 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---------------------------------|--------------------------------------|----------------|-----|--------|-----------------|
| V _{CC} | Analog supply voltage | 4.5 | 5 | 5.5 | V |
| V _{DD} | Digital supply voltage | 2.7 | 3.3 | 3.6 | V |
| Digital input interface level | | TTL compatible | | | |
| Digital input clock frequency | Sampling frequency, LRCK1, LRCK2 | 16 | | 96/192 | kHz |
| | System clock frequency, SCKI1, SCKI2 | 2.048 | | 36.864 | MHz |
| Analog input level | | 3 | | | V _{pp} |
| Analog output load resistance | AC-coupled | 5 | | | kΩ |
| | DC-coupled | 10 | | | kΩ |
| Analog output load capacitance | | 50 | | | pF |
| Digital output load capacitance | | 20 | | | pF |
| Operating free-air temperature | | -25 | 25 | 85 | °C |

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCKI1} = \text{SCKI2} = 512\text{ f}_S$, 24-bit data (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | PCM3060PW | | | UNIT | | |
|---|---|---|---------------------|-------|-----------------|----------|-----|
| | | MIN | TYP | MAX | | | |
| DIGITAL INPUT/OUTPUT | | | | | | | |
| DATA FORMAT | | | | | | | |
| Audio data interface format | | I ² S, LJ, RJ | | | | | |
| Audio data word length | | 16, 24 | | | Bits | | |
| Audio data format | | MSB-first, 2s-complement | | | | | |
| f _S | Sampling frequency, ADC | 16 | 48 | 96 | kHz | | |
| | Sampling frequency, DAC | 16 | 48 | 192 | | | |
| | System clock frequency | 128, 192, 256, 384, 512, 768 f _S | | 2.048 | 36.864 | MHz | |
| INPUT LOGIC | | | | | | | |
| V _{IH} ⁽¹⁾ | Input logic level | | 2 | | V _{DD} | VDC | |
| V _{IL} ⁽¹⁾ | | | | | 0.8 | | |
| V _{IH} ^{(2) (3)} | | | 2 | | | | 5.5 |
| V _{IL} ^{(2) (3)} | | | | | | | 0.8 |
| I _{IH} ⁽²⁾ | Input logic current | V _{IN} = V _{DD} | | | | ±10 | |
| I _{IL} ⁽²⁾ | | V _{IN} = 0 V | | | | ±10 | |
| I _{IH} ^{(1) (3)} | | V _{IN} = V _{DD} | | 65 | | 100 | |
| I _{IL} ^{(1) (3)} | | V _{IN} = 0 V | | | | ±10 | |
| OUTPUT LOGIC | | | | | | | |
| V _{OH} ⁽⁴⁾ | Output logic level | I _{OUT} = -4 mA | 2.8 | | | VDC | |
| V _{OL} ^{(4) (5)} | | I _{OUT} = 4 mA | | | 0.5 | | |
| REFERENCE OUTPUT | | | | | | | |
| V _{COM} output voltage | | | 0.5 V _{CC} | | | V | |
| V _{COM} output impedance | | | 7 | 12.5 | 18 | kΩ | |
| Allowable V _{COM} output source/sink current | | | | | ±1 | μA | |
| ADC CHARACTERISTICS | | | | | | | |
| Resolution | | | 16 | 24 | | Bits | |
| ANALOG INPUT | | | | | | | |
| Full scale input voltage | V _{INL} , V _{INR} = 0 dB | | 0.6 V _{CC} | | | Vp-p | |
| Center voltage | | | 0.5 V _{CC} | | | V | |
| Input impedance | | | 10 | | | kΩ | |
| Antialiasing filter response | -3 dB | | 300 | | | kHz | |
| DC ACCURACY | | | | | | | |
| Gain mismatch, channel-to-channel | Full-scale input, V _{INL} , V _{INR} | | ±2 | ±8 | | % of FSR | |
| Gain error | Full-scale input, V _{INL} , V _{INR} | | ±2 | ±8 | | % of FSR | |
| Bipolar zero error | HPF bypass, V _{INL} , V _{INR} | | ±0.5 | ±2 | | % of FSR | |

- (1) BCK1, BCK2, LRCK1, LRCK2 (in slave mode, Schmitt-trigger input with 50-kΩ typical internal pulldown resistor)
- (2) SCKI1, SCKI2, DIN, $\overline{\text{MS}}/\text{ADR}/\text{IFMD}$, MC/SCL/FMT, MD/SDA/IFMD (Schmitt-trigger input, 5-V tolerant).
- (3) $\overline{\text{RST}}$ (Schmitt-trigger input with 50-kΩ typical internal pulldown resistor, 5-V tolerant).
- (4) BCK1, BCK2, LRCK1, LRCK2 (in master mode), DOUT, ZEROL, ZEROR
- (5) MD/SDA/IFMD (in I²C mode, open drain LOW output)

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCK11} = \text{SCK12} = 512 f_S$, 24-bit data (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | PCM3060PW | | | UNIT |
|--|--|---|---------------|--------------------|------------|
| | | MIN | TYP | MAX | |
| DYNAMIC PERFORMANCE ⁽⁶⁾ ⁽⁷⁾ | | | | | |
| THD+N | Total harmonic distortion + noise | $V_{IN} = -1\text{ dB}$, $f_S = 48\text{ kHz}$ | -93 | -85 | dB |
| | | $V_{IN} = -1\text{ dB}$, $f_S = 96\text{ kHz}$ | -93 | | |
| Dynamic range | | $f_S = 48\text{ kHz}$, A-weighted | 95 | 99 | dB |
| | | $f_S = 96\text{ kHz}$, A-weighted | | 101 | |
| SNR | Signal-to-noise ratio | $f_S = 48\text{ kHz}$, A-weighted | 95 | 99 | dB |
| | | $f_S = 96\text{ kHz}$, A-weighted | | 101 | |
| Channel separation (between L-ch and R-ch) | | $f_S = 48\text{ kHz}$ | 92 | 96 | dB |
| | | $f_S = 96\text{ kHz}$ | | 98 | |
| Crosstalk from DAC | | $f_{S1} = 48\text{ kHz}$, $f_{S2} = 44.1\text{ kHz}$ | 92 | 96 | dB |
| | | $f_{S1} = 96\text{ kHz}$, $f_{S2} = 44.1\text{ kHz}$ | | 98 | |
| DIGITAL FILTER PERFORMANCE | | | | | |
| Pass band | | | | $0.454 f_S$ | Hz |
| Stop band | | | $0.583 f_S$ | | Hz |
| Pass-band ripple | $< 0.454 f_S$ | | | ± 0.05 | dB |
| Stop-band attenuation | $> 0.583 f_S$ | | -65 | | dB |
| Group delay time | | | | $17.4/f_S$ | s |
| HPF frequency response | -3 dB | | | $0.019 f_S / 1000$ | Hz |
| DAC CHARACTERISTICS | | | | | |
| Resolution | | 16 | 24 | | Bits |
| ANALOG OUTPUT | | | | | |
| Output voltage | Single-ended | | $0.8 V_{CC}$ | | Vp-p |
| | Differential | | $1.6 V_{CC}$ | | |
| Center voltage | Single-ended | | $0.5 V_{CC}$ | | V |
| | Differential | | $0.48 V_{CC}$ | | |
| Load impedance | AC-coupled | 5 | | | k Ω |
| | DC-coupled | 10 | | | |
| LPF frequency response | $f = 20\text{ kHz}$ | | -0.02 | | dB |
| | $f = 44\text{ kHz}$ | | -0.07 | | |
| | -3 dB | | | 300 | kHz |
| DC ACCURACY | | | | | |
| Gain mismatch, channel-to-channel | | | ± 1 | ± 4 | % of FSR |
| Gain error | | | ± 2 | ± 6 | % of FSR |
| Bipolar zero error | Single-ended | | ± 1 | ± 2 | % of FSR |
| | Differential ($V_{OUTX+} - V_{OUTX-}$) | | ± 1 | | |

(6) $f_{IN} = 1\text{ kHz}$, using System Two audio measurement system by Audio Precision, RMS mode with 20-kHz LPF and 400-Hz HPF.

(7) $f_S = 96\text{ kHz}$: $\text{SCK11} = \text{SCK12} = 256 f_S$, $f_S = 192\text{ kHz}$: $\text{SCK11} = 512 f_S$ at $f_S = 48\text{ kHz}$ and $\text{SCK12} = 128 f_S$ at $f_S = 192\text{ kHz}$.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCKI1} = \text{SCKI2} = 512 f_S$, 24-bit data (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | PCM3060PW | | | UNIT |
|---|-----------------------------------|--|----------------|----------------|------------|------|
| | | | MIN | TYP | MAX | |
| DYNAMIC PERFORMANCE (SINGLE-ENDED) ⁽⁸⁾ ⁽⁹⁾ ⁽¹⁰⁾ | | | | | | |
| THD+N | Total harmonic distortion + noise | $V_{OUT} = 0\text{ dB}$, $f_S = 48\text{ kHz}$ | | –93 | –85 | dB |
| | | $V_{OUT} = 0\text{ dB}$, $f_S = 96\text{ kHz}$ | | –94 | | |
| | | $V_{OUT} = 0\text{ dB}$, $f_S = 192\text{ kHz}$ | | –94 | | |
| Dynamic range | | $f_S = 48\text{ kHz}$, EIAJ, A-weighted | 99 | 103 | | dB |
| | | $f_S = 96\text{ kHz}$, EIAJ, A-weighted | | 103 | | |
| | | $f_S = 192\text{ kHz}$, EIAJ, A-weighted | | 103 | | |
| SNR | Signal-to-noise ratio | $f_S = 48\text{ kHz}$, EIAJ, A-weighted | 100 | 104 | | dB |
| | | $f_S = 96\text{ kHz}$, EIAJ, A-weighted | | 104 | | |
| | | $f_S = 192\text{ kHz}$, EIAJ, A-weighted | | 104 | | |
| Channel separation | | $f_S = 48\text{ kHz}$ | 97 | 101 | | dB |
| | | $f_S = 96\text{ kHz}$ | | 101 | | |
| | | $f_S = 192\text{ kHz}$ | | 101 | | |
| Crosstalk from ADC | | $f_{S1} = 48\text{ kHz}$, $f_{S2} = 44.1\text{ kHz}$ | 97 | 101 | | dB |
| | | $f_{S1} = 48\text{ kHz}$, $f_{S2} = 88.2\text{ kHz}$ | | 101 | | |
| | | $f_{S1} = 48\text{ kHz}$, $f_{S2} = 176.4\text{ kHz}$ | | 101 | | |
| DYNAMIC PERFORMANCE (DIFFERENTIAL) ⁽⁸⁾ ⁽⁹⁾ ⁽¹¹⁾ | | | | | | |
| THD+N | Total harmonic distortion + noise | $V_{OUT} = 0\text{ dB}$, $f_S = 48\text{ kHz}$ | | –94 | | dB |
| | | $V_{OUT} = 0\text{ dB}$, $f_S = 96\text{ kHz}$ | | –95 | | |
| | | $V_{OUT} = 0\text{ dB}$, $f_S = 192\text{ kHz}$ | | –95 | | |
| Dynamic range | | $f_S = 48\text{ kHz}$, EIAJ, A-weighted | | 104 | | dB |
| | | $f_S = 96\text{ kHz}$, EIAJ, A-weighted | | 104 | | |
| | | $f_S = 192\text{ kHz}$, EIAJ, A-weighted | | 104 | | |
| SNR | Signal-to-noise ratio | $f_S = 48\text{ kHz}$, EIAJ, A-weighted | | 105 | | dB |
| | | $f_S = 96\text{ kHz}$, EIAJ, A-weighted | | 105 | | |
| | | $f_S = 192\text{ kHz}$, EIAJ, A-weighted | | 105 | | |
| Channel separation | | $f_S = 48\text{ kHz}$ | | 103 | | dB |
| | | $f_S = 96\text{ kHz}$ | | 103 | | |
| | | $f_S = 192\text{ kHz}$ | | 103 | | |
| Crosstalk from ADC | | $f_{S1} = 48\text{ kHz}$, $f_{S2} = 44.1\text{ kHz}$ | | 103 | | dB |
| | | $f_{S1} = 48\text{ kHz}$, $f_{S2} = 88.2\text{ kHz}$ | | 103 | | |
| | | $f_{S1} = 48\text{ kHz}$, $f_{S2} = 176.4\text{ kHz}$ | | 103 | | |
| DIGITAL FILTER PERFORMANCE SHARP ROLLOFF | | | | | | |
| Pass band | | | | 0.454 f_S | | Hz |
| Stop band | | | 0.546 f_S | | | Hz |
| Pass-band ripple | $< 0.454 f_S$ | | | | ± 0.04 | dB |
| Stop-band attenuation | $> 0.546 f_S$ | | –50 | | | dB |

(8) $f_S = 96\text{ kHz}$: $\text{SCKI1} = \text{SCKI2} = 256 f_S$, $f_S = 192\text{ kHz}$: $\text{SCKI1} = 512 f_S$ at $f_S = 48\text{ kHz}$ and $\text{SCKI2} = 128 f_S$ at $f_S = 192\text{ kHz}$.

(9) $f_{OUT} = 1\text{ kHz}$, using System Two audio measurement system by Audio Precision, RMS mode with 20-kHz LPF and 400-Hz HPF.

(10) Assumed 5-k Ω AC-coupled second-order LPF and 115-dB or higher- performance buffer.

(11) Assumed 10-k Ω DC-coupled second-order LPF and 115- dB or higher-performance differential to single-ended converter.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCK11} = \text{SCK12} = 512 f_S$, 24-bit data (unless otherwise noted).

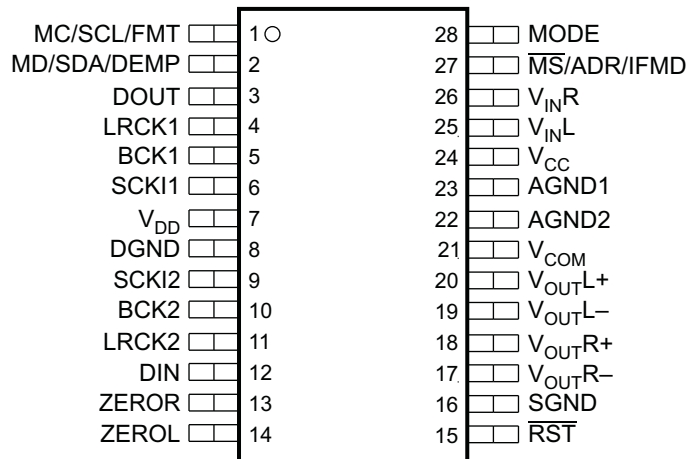
| PARAMETER | | TEST CONDITIONS | PCM3060PW | | | UNIT |
|-----------------------------------|-----------------------|--|------------|-----------|----------------|--------------------|
| | | | MIN | TYP | MAX | |
| DIGITAL FILTER PERFORMANCE | | SLOW ROLLOFF | | | | |
| | Pass band | | | | 0.308 f_S | Hz |
| | Stop band | | 0.73 f_S | | | Hz |
| | Pass-band ripple | $< 0.308 f_S$ | | | ± 0.5 | dB |
| | Stop-band attenuation | $> 0.73 f_S$ | -35 | | | dB |
| DIGITAL FILTER PERFORMANCE | | | | | | |
| | Group delay time | | | 20/ f_S | | s |
| | De-emphasis error | | | ± 0.1 | | dB |
| POWER SUPPLY REQUIREMENTS | | | | | | |
| V_{CC} | Voltage range | | 4.5 | 5 | 5.5 | VDC |
| V_{DD} | | | 2.7 | 3.3 | 3.6 | |
| I_{CC} | Supply current | $f_S = 48\text{ kHz/ADC}$, $f_S = 48\text{ kHz/DAC}$ | | 25 | 36 | mA |
| | | $f_S = 96\text{ kHz/ADC}$, $f_S = 96\text{ kHz/DAC}$ | | 25 | | mA |
| | | $f_{S1} = 48\text{ kHz/ADC}$, $f_{S2} = 192\text{ kHz/DAC}$ | | 25 | | mA |
| | | $f_S = 48\text{ kHz/ADC}$, power down/DAC | | 12 | | mA |
| | | Power down/ADC, $f_S = 48\text{ kHz/DAC}$ | | 13 | | mA |
| | | Full power down ⁽¹²⁾ ⁽¹³⁾ | | 780 | | μA |
| I_{DD} | Supply current | $f_S = 48\text{ kHz/ADC}$, $f_S = 48\text{ kHz/DAC}$ | | 9 | 12 | mA |
| | | $f_S = 96\text{ kHz/ADC}$, $f_S = 96\text{ kHz/DAC}$ | | 16 | | mA |
| | | $f_{S1} = 48\text{ kHz/ADC}$, $f_{S2} = 192\text{ kHz/DAC}$ | | 13 | | mA |
| | | $f_S = 48\text{ kHz/ADC}$, power down/DAC | | 5 | | mA |
| | | Power down/ADC, $f_S = 48\text{ kHz/DAC}$ | | 5 | | mA |
| | | Full power down ⁽¹²⁾ | | 150 | | μA |
| Power dissipation | | $f_S = 48\text{ kHz/ADC}$, $f_S = 48\text{ kHz/DAC}$ | | 160 | 220 | mW |
| | | $f_S = 96\text{ kHz/ADC}$, $f_S = 96\text{ kHz/DAC}$ | | 180 | | |
| | | $f_{S1} = 48\text{ kHz/ADC}$, $f_{S2} = 192\text{ kHz/DAC}$ | | 170 | | |
| | | $f_S = 48\text{ kHz/ADC}$, power down/DAC | | 77 | | |
| | | Power down/ADC, $f_S = 48\text{ kHz/DAC}$ | | 82 | | |
| | | Full power down ⁽¹²⁾ ⁽¹³⁾ | | 4.4 | | |
| TEMPERATURE RANGE | | | | | | |
| | Operation temperature | | -25 | | 85 | $^\circ\text{C}$ |
| θ_{JA} | Thermal resistance | | | 105 | | $^\circ\text{C/W}$ |

(12) Halt SCK11, SCK12, BCK1, BCK2, LRCK1, LRCK2

(13) AC-coupled configuration. If DC-coupled configuration is used, DC current flow to external load is added and it depends on external load resistance.

PIN ASSIGNMENTS

PCM3060
PW (TSSOP) PACKAGE
(TOP VIEW)



P0043-03

Table 1. TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---------------------------|-----|--------------------|--|
| NAME | PIN | | |
| AGND1 | 23 | – | ADC analog ground |
| AGND2 | 22 | – | DAC analog ground |
| BCK1 | 5 | I/O ⁽¹⁾ | Audio data bit clock input/output for ADC |
| BCK2 | 10 | I/O ⁽¹⁾ | Audio data bit clock input/output for DAC |
| DGND | 8 | – | Digital ground |
| DIN | 12 | I ⁽²⁾ | Audio data digital input for DAC |
| DOUT | 3 | O | Audio data digital output for ADC |
| LRCK1 | 4 | I/O ⁽¹⁾ | Audio data left/right clock input/output for ADC |
| LRCK2 | 11 | I/O ⁽¹⁾ | Audio data left/right clock input/output for DAC |
| MC/SCL/FMT | 1 | I ⁽²⁾ | Mode control, clock for SPI, clock for I ² C, format for H/W mode ⁽⁵⁾ |
| MD/SDA/DEMP | 2 | I/O ⁽³⁾ | Mode control, data for SPI, data for I ² C, de-emphasis for H/W mode |
| MODE | 28 | I ⁽⁴⁾ | This pin provides four operation modes according to its input connection. Connected directly to V _{DD} : SPI mode. Connected to V _{DD} through 220-k Ω pullup resistor: H/W mode, single-ended V _{OUTX} . Connected to DGND through 220-k Ω pulldown resistor: H/W mode, differential V _{OUTX} . Connected directly to DGND : I ² C mode. |
| \overline{MS} /ADR/IFMD | 27 | I ⁽²⁾ | Mode control, select for SPI with low active, address for I ² C, I/F mode for H/W mode |
| RST | 15 | I ⁽⁵⁾ | Reset and power-down control input, active-low |
| SCK1 | 6 | I ⁽²⁾ | System clock input for ADC |
| SCK2 | 9 | I ⁽²⁾ | System clock input for DAC |
| SGND | 16 | – | Shield analog ground |
| V _{CC} | 24 | – | ADC, DAC analog power supply, 5-V |
| V _{COM} | 21 | – | ADC, DAC voltage common decoupling |
| V _{DD} | 7 | – | Digital power supply, 3.3-V |
| V _{INL} | 25 | I | Analog input to ADC, L-channel |
| V _{INR} | 26 | I | Analog input to ADC, R-channel |
| V _{OUTL} – | 19 | O | Analog output from DAC, L-channel – in differential mode, must be open in single-ended mode |
| V _{OUTL} + | 20 | O | Analog output from DAC, L-channel + in differential mode, L-channel in single-ended mode |
| ZEROL | 14 | O | Zero flag, L-channel |
| ZEROR | 13 | O | Zero flag, R-channel |
| V _{OUTR} – | 17 | O | Analog output from DAC, R-channel – in differential mode, must be open in single-ended mode |
| V _{OUTR} + | 18 | O | Analog output from DAC, R-channel + in differential mode, R-channel in single-ended mode |

(1) Schmitt-trigger input/output with 50-k Ω typical internal pulldown resistor

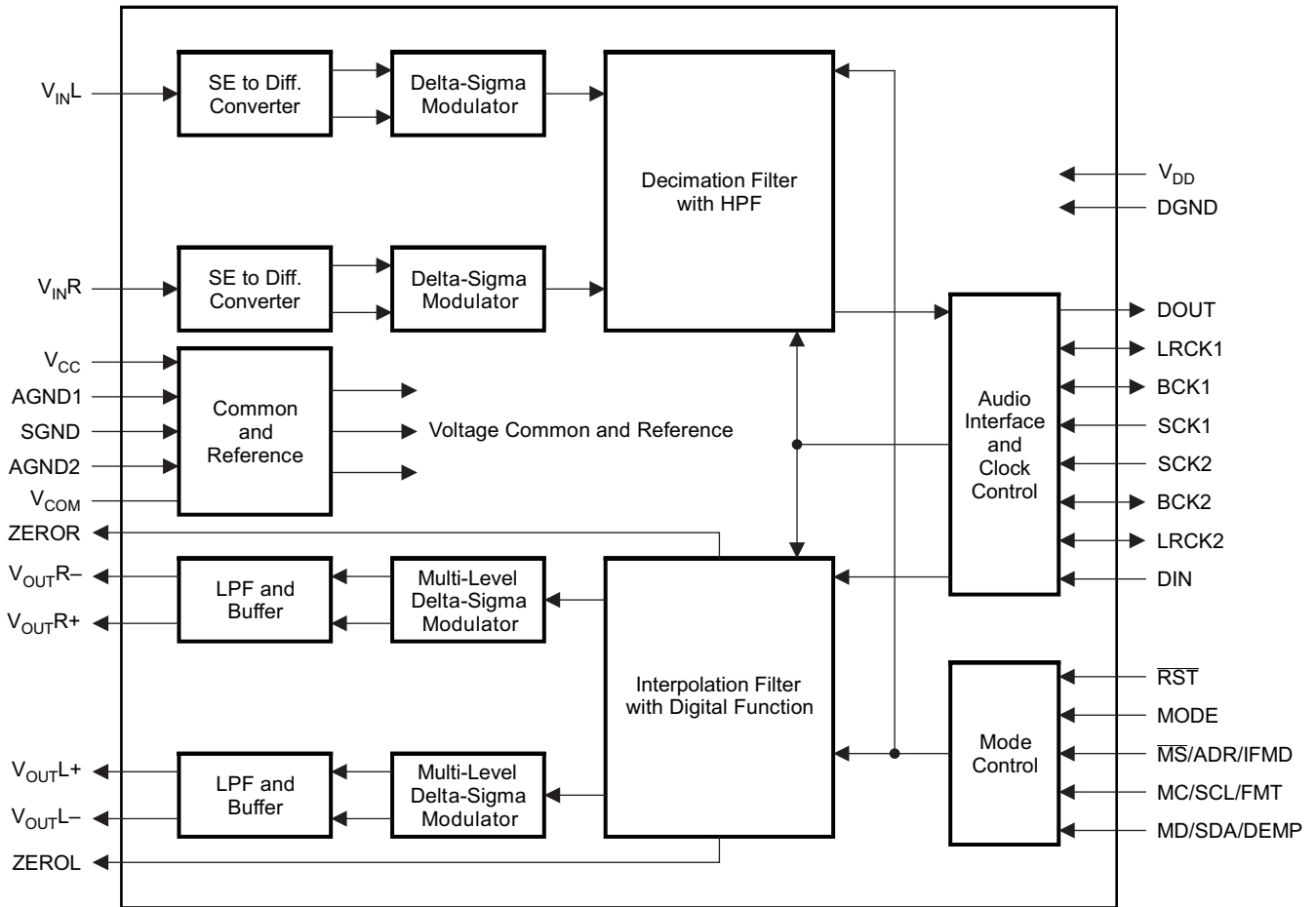
(2) Schmitt-trigger input, 5-V tolerant

(3) Schmitt-trigger input, 5 V tolerant for SPI, H/W mode and Schmitt-trigger input/open drain LOW output, 5-V tolerant for I²C

(4) V_{DD}/2 biased, quad-state input

(5) Schmitt-trigger input with 50-k Ω typical internal pulldown resistor, 5-V tolerant

BLOCK DIAGRAM



B0229-01

TYPICAL PERFORMANCE CURVES OF ADC INTERNAL FILTER

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCK11} = \text{SCK12} = 512\text{ f}_S$, 24-bit data, unless otherwise noted.

DIGITAL FILTER

DECIMATION FILTER, STOP-BAND CHARACTERISTICS

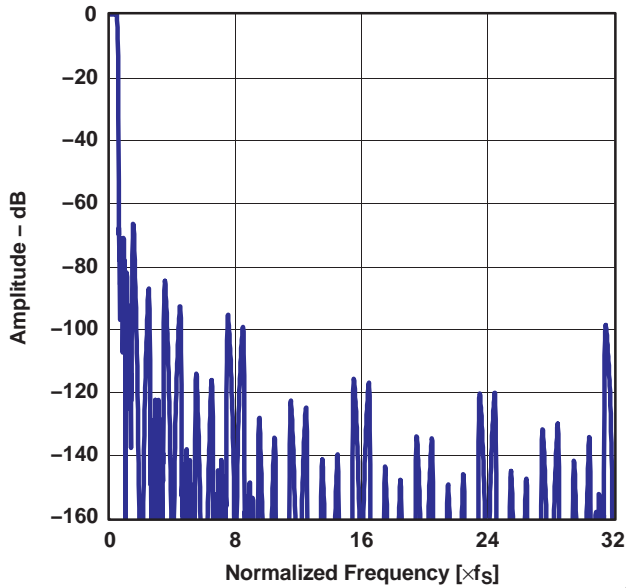


Figure 1.

DECIMATION FILTER, PASS-BAND CHARACTERISTICS

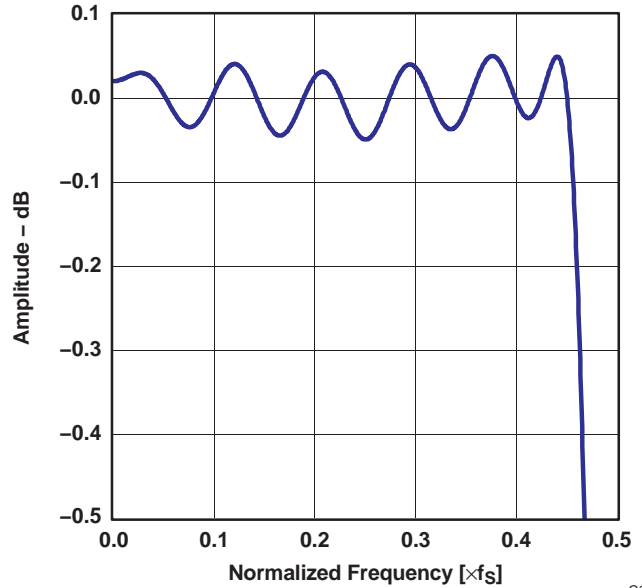


Figure 2.

ANALOG FILTER

HIGH-PASS FILTER CHARACTERISTICS

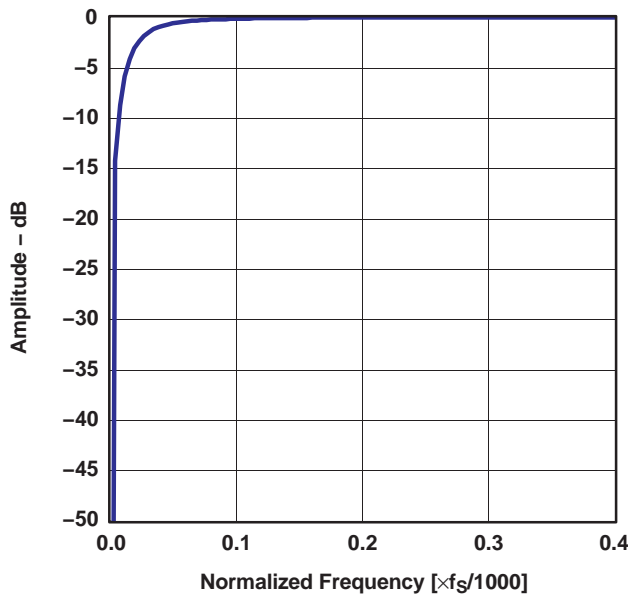


Figure 3.

ANTI_ALIASING FILTER CHARACTERISTICS

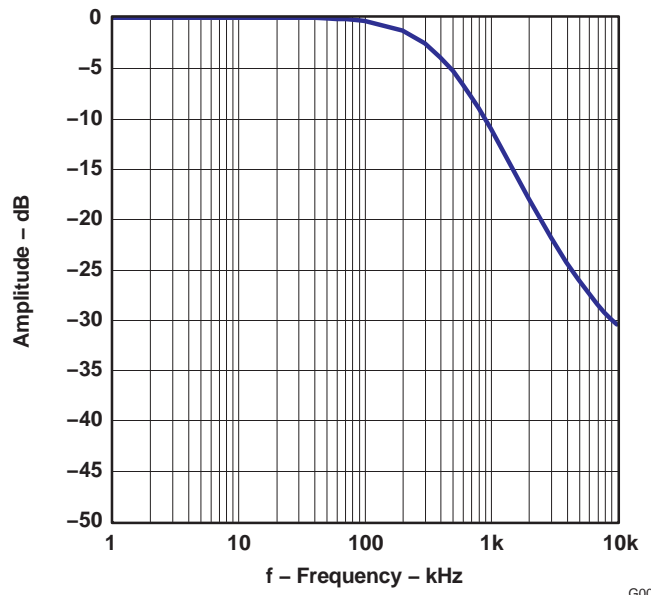


Figure 4.

TYPICAL PERFORMANCE CURVES OF DAC INTERNAL FILTER

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCK11} = \text{SCK12} = 512 f_S$, 24-bit data, unless otherwise noted.

DIGITAL FILTER

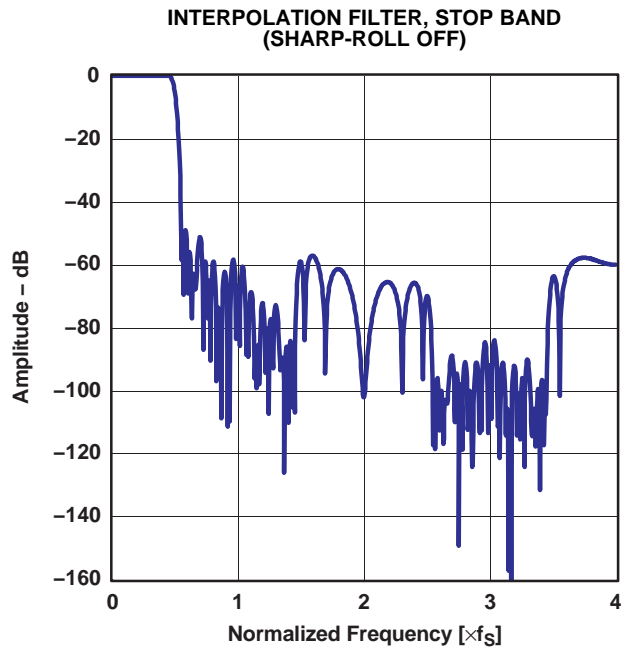


Figure 5.

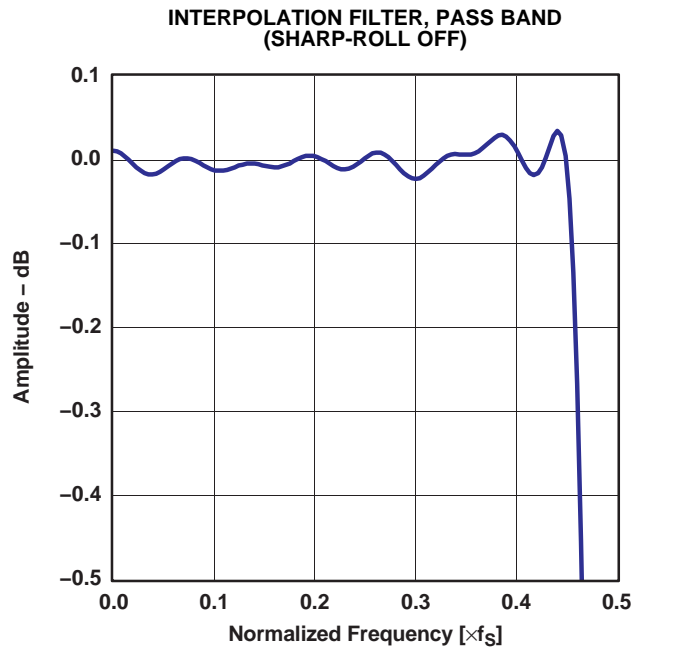


Figure 6.

ANALOG FILTER

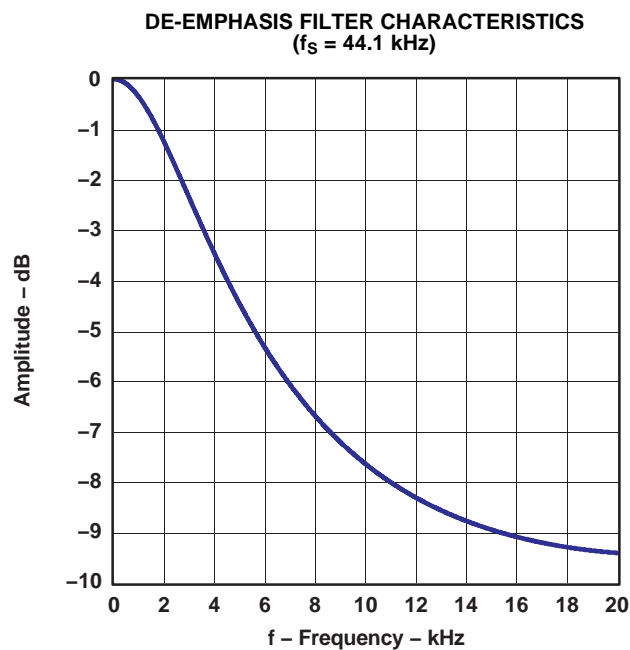


Figure 7.

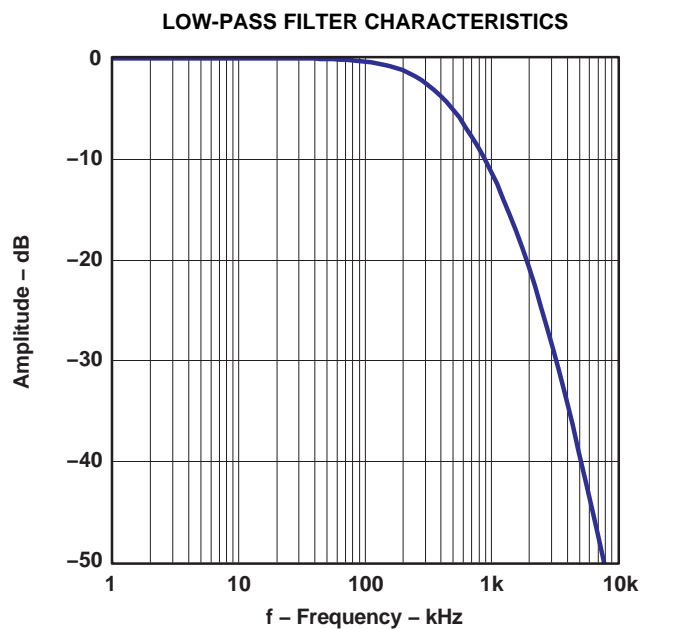


Figure 8.

TYPICAL ADC PERFORMANCE CURVES

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCK11} = \text{SCK12} = 512\text{ f}_S$, 24-bit data, unless otherwise noted.

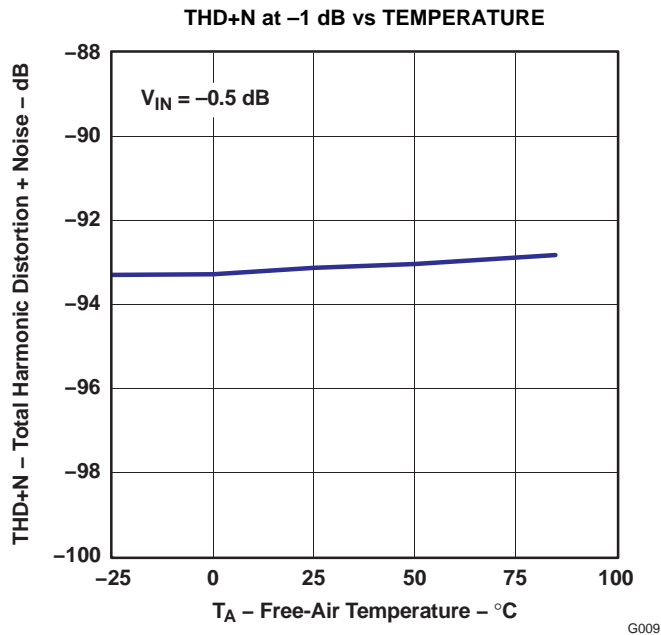


Figure 9.

G009

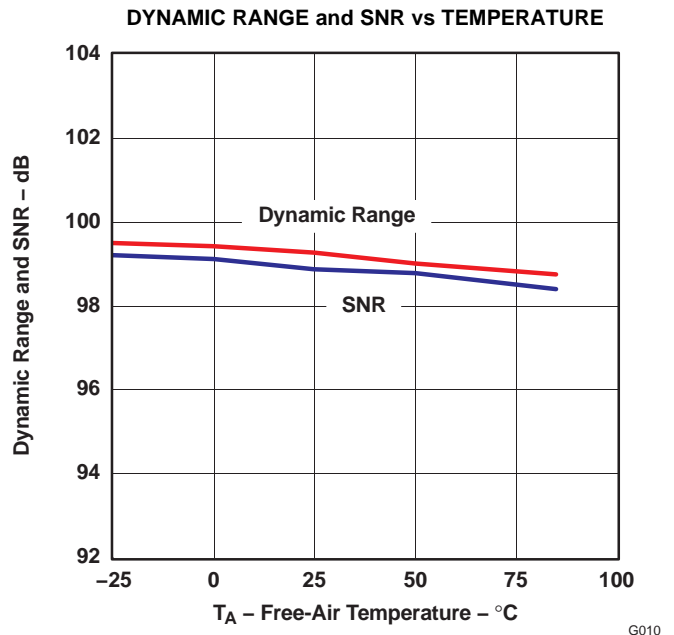


Figure 10.

G010

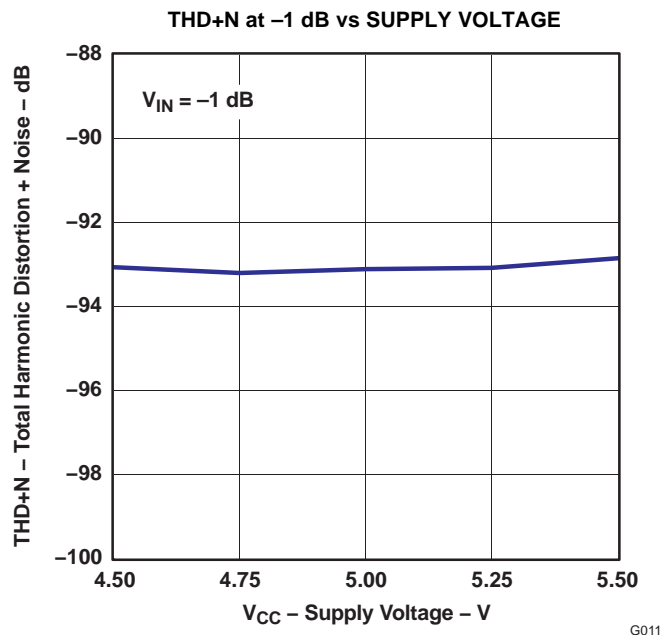


Figure 11.

G011

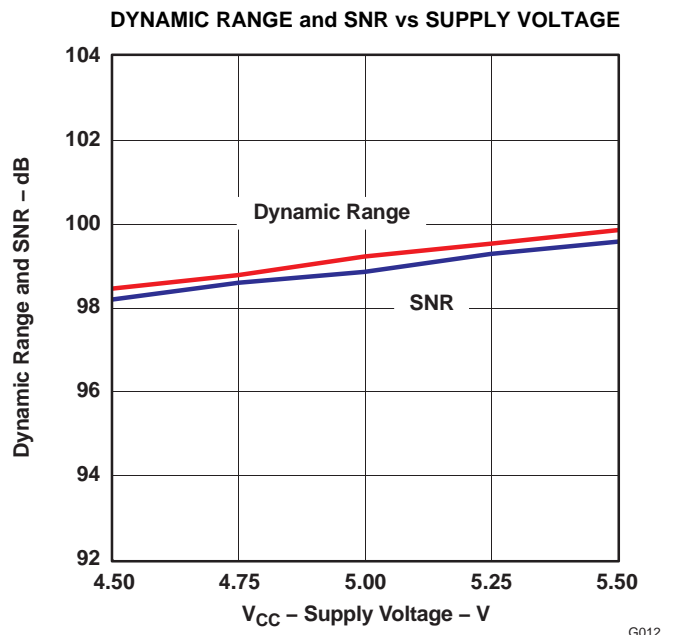


Figure 12.

G012

TYPICAL DAC PERFORMANCE CURVES

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCKI1} = \text{SCKI2} = 512 f_S$, 24-bit data, unless otherwise noted.

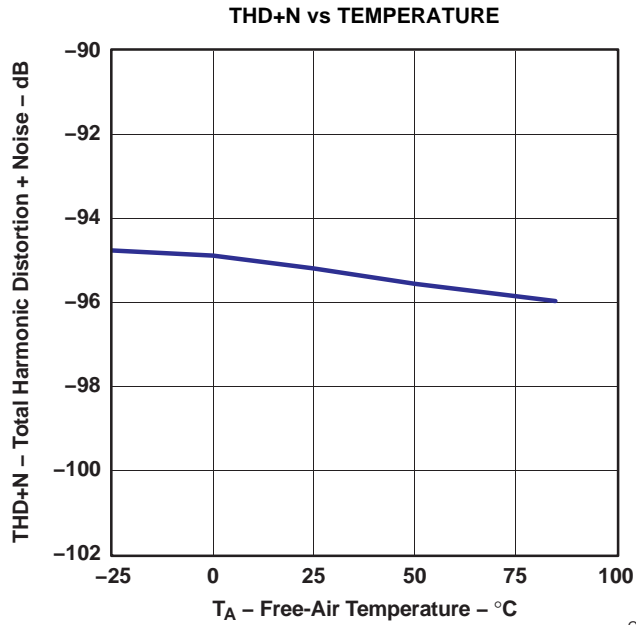


Figure 13.

G013

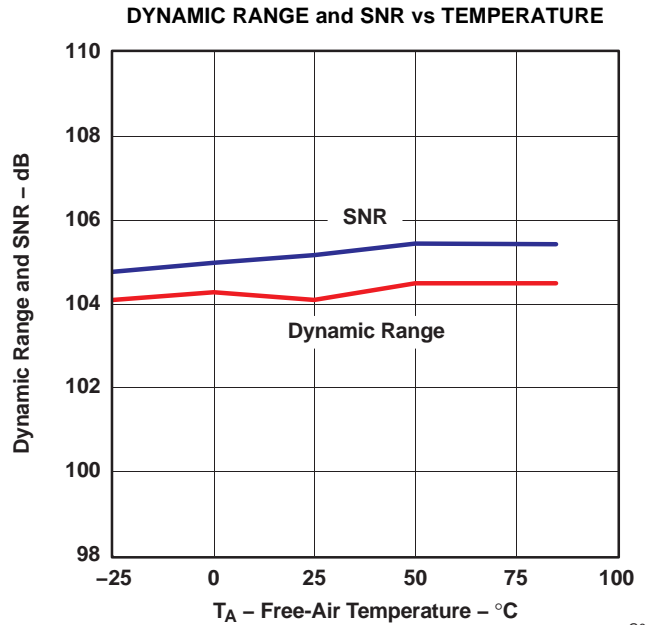


Figure 14.

G014

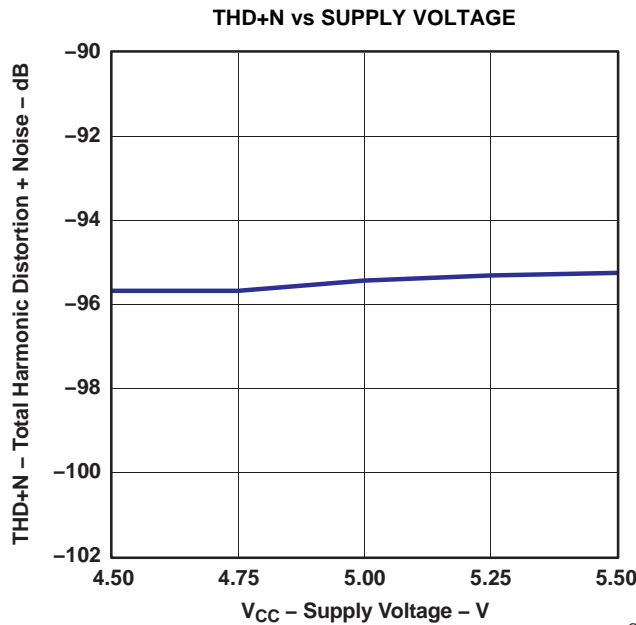


Figure 15.

G015

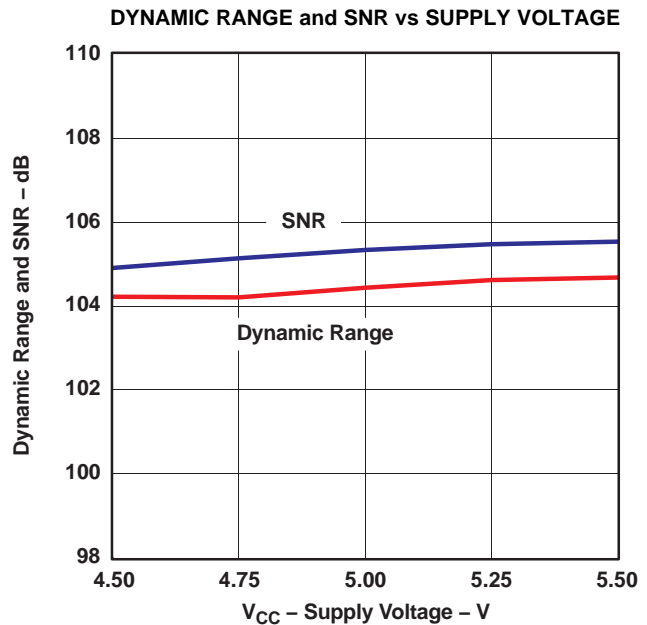


Figure 16.

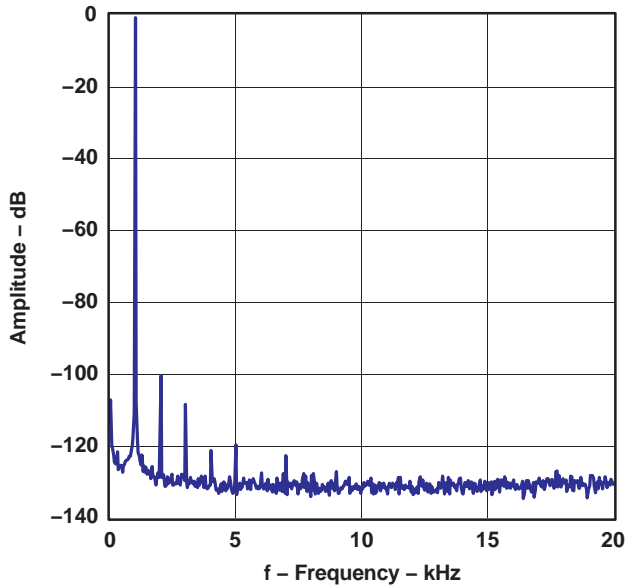
G016

TYPICAL PERFORMANCE CURVES

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, $\text{SCKI1} = \text{SCKI2} = 512\text{ f}_S$, 24-bit data, unless otherwise noted.

ADCs OUTPUT SPECTRUM

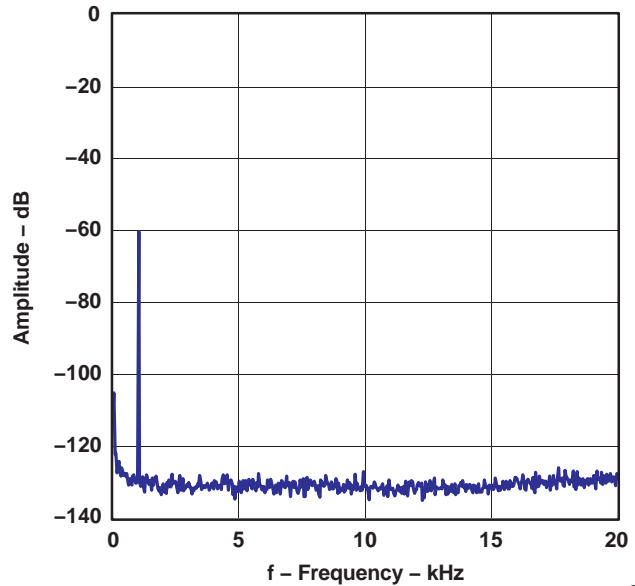
OUTPUT SPECTRUM (-1 dB, N=32768)



G017

Figure 17.

OUTPUT SPECTRUM (-60 dB, N=32768)

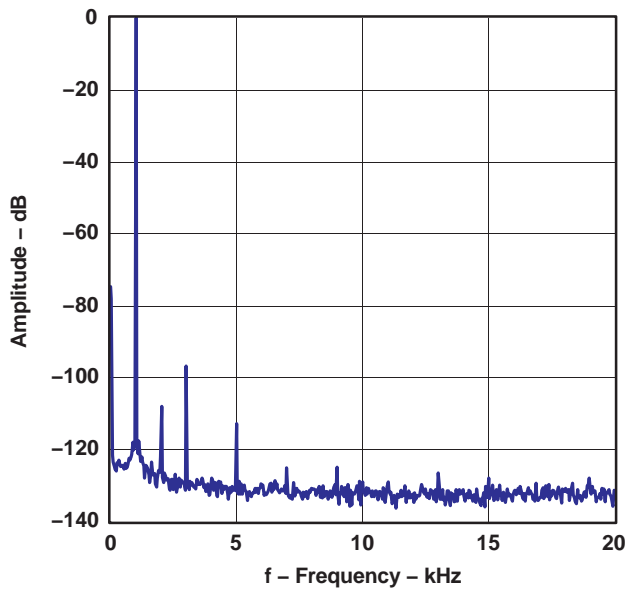


G018

Figure 18.

DAC OUTPUT SPECTRUM

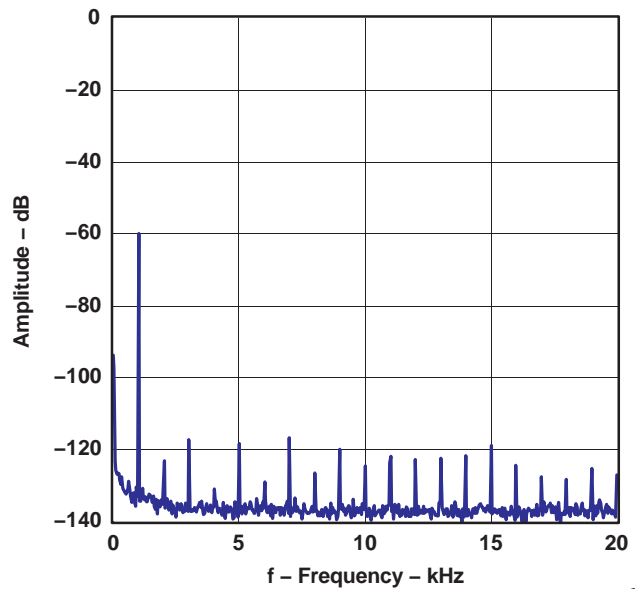
OUTPUT SPECTRUM (0 dB, N=32768)



G019

Figure 19.

OUTPUT SPECTRUM (-60 dB, N=32768)



G020

Figure 20.

DEVICE DESCRIPTION

ASYNCHRONOUS OPERATION

The PCM3060 supports complete asynchronous operation between the ADC and DAC by receiving two independent system clocks on SCK11 and SCK12.

Also, the PCM3060 supports synchronous operation between ADC and DAC by receiving one common system clock on either SCK11 or SCK12 and controlling the system clock configuration through register 67 or 72 in serial mode control.

SYSTEM CLOCK

The PCM3060 requires two system clocks for operating the ADC and DAC blocks independently, or it requires one common clock for synchronous ADC and DAC operation.

The system clock for the ADC of the PCM3060 must be 256, 384, 512, or 768 f_s , where f_s is the audio sampling rate for the ADC, 16 to 96 kHz.

The system clock for the DAC of the PCM3060 must be 128, 192, 256, 384, 512, or 768 f_s , where f_s is the audio sampling rate for the DAC, 16 to 192 kHz.

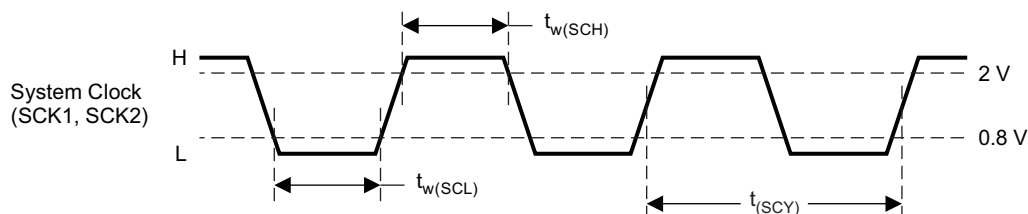
Table 2 lists the typical system clock frequencies, f_{SCK11} and f_{SCK12} for common audio sampling rates, and Figure 21 shows the timing requirements for the system clock inputs.

Table 2. System Clock Frequencies for Common Audio Sampling Clock Frequencies

| SAMPLING FREQUENCY (kHz) | SYSTEM CLOCK FREQUENCY, f_{SCK11} , f_{SCK12} [MHz] | | | | | |
|--------------------------|---|--------------------------|--------------------|--------------------|--------------------|--------------------|
| | 128 f_s ⁽¹⁾ | 192 f_s ⁽¹⁾ | 256 f_s | 384 f_s | 512 f_s | 768 f_s |
| 16 | 2.048 | 3.072 | 4.096 | 6.144 | 8.192 | 12.288 |
| 32 | 4.096 | 6.144 | 8.192 | 12.288 | 16.384 | 24.576 |
| 44.1 | 5.6488 | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 48 | 6.144 | 9.216 | 12.288 | 18.432 | 24.576 | 36.864 |
| 88.2 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | See ⁽²⁾ | See ⁽²⁾ |
| 96 | 12.288 | 18.432 | 24.576 | 36.864 | See ⁽²⁾ | See ⁽²⁾ |
| 176.4 ⁽¹⁾ | 22.5792 | 33.8688 | See ⁽²⁾ | See ⁽²⁾ | See ⁽²⁾ | See ⁽²⁾ |
| 192 ⁽¹⁾ | 24.576 | 36.864 | See ⁽²⁾ | See ⁽²⁾ | See ⁽²⁾ | See ⁽²⁾ |

(1) This combination of sampling clock frequency and system clock frequency is supported only for the DAC.

(2) This system clock frequency is not supported for the given sampling clock frequency.



T0005-14

| SYMBOL | PARAMETERS | MIN | MAX | UNIT |
|--------------|-------------------------|-----------------|-----|------|
| $t_{(SCY)}$ | System clock cycle time | 25 | | ns |
| $t_{w(SCH)}$ | System clock high time | 0.4 $t_{(SCY)}$ | | ns |
| $t_{w(SCL)}$ | System clock low time | 0.4 $t_{(SCY)}$ | | ns |
| | System clock duty cycle | 40% | 60% | |

Figure 21. System Clock Input Timing

POWER-ON RESET AND EXTERNAL RESET SEQUENCE

The PCM3060 has both an internal power-on reset circuit and an external reset circuit. The sequences for both resets are shown in the following.

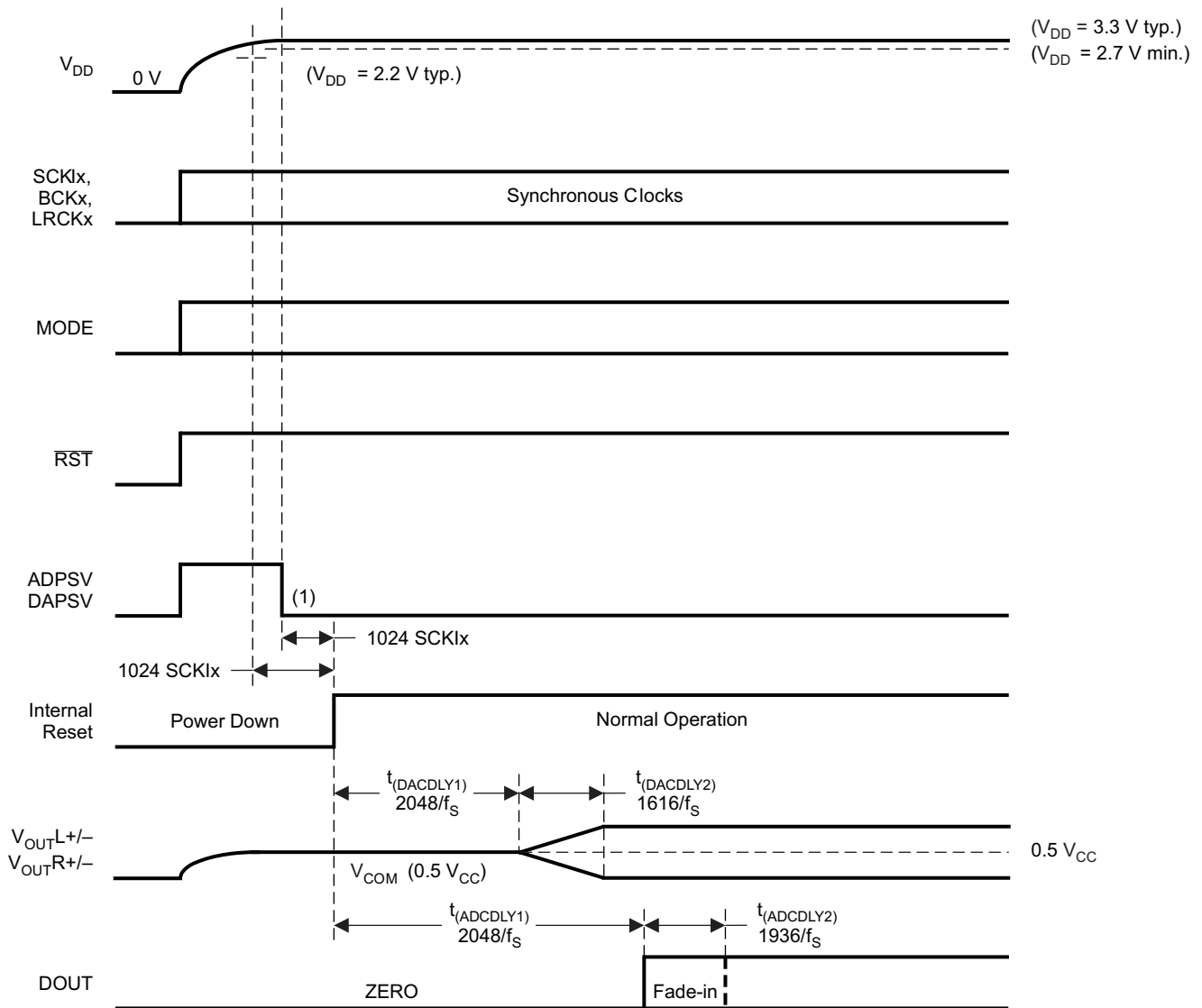
Figure 22 illustrates the timing of the internal power-on reset. Initialization (reset) is done automatically at the time when V_{DD} exceeds 2.2 V typical.

Internal reset is released 1024 SCKIx ($x = 1, 2$) after power on if the H/W control mode is selected and \overline{RST} is kept HIGH; then the PCM3060 begins normal operation. If the S/W control mode is selected and \overline{RST} is kept HIGH, internal reset is released 1024 SCKIx after the reset of ADPSV and DAPSV through serial control port; then the PCM3060 begins normal operation. If \overline{RST} is kept LOW, internal reset is held and the reset sequence is frozen until \overline{RST} is changed from LOW to HIGH. V_{OUTL} and V_{OUTR} from the DAC are forced to the V_{COM} ($= 0.5 V_{CC}$) level as V_{CC} rises. If synchronization is maintained among SCKIx, BCKx, and LRCKx, V_{OUTL} and V_{OUTR} go into the fade-in sequence after $t_{DACDLY1} = 2048/f_S$ from internal reset release. Then V_{OUTL} and V_{OUTR} provide outputs corresponding to DIN after $t_{DACDLY2} = 1616/f_S$ from the start of fade-in. Similarly, DOUT from the ADC is enabled and goes into the fade-in sequence after $t_{ADCDLY1} = 2048/f_S$ from internal reset release, and then DOUT provides an output corresponding to V_{INL} and V_{INR} after $t_{ADCDLY2} = 1936/f_S$ from the start of fade-in. If synchronization is not held, the internal reset is not released and operation mode is kept on reset and power-down state. After resynchronization, the DAC begins its fade-in sequence, and the ADC also begins fade-in operation after internal initialization and an initial delay.

Figure 23 is the timing chart of the external reset. The \overline{RST} pin initiates external forced reset when \overline{RST} is held LOW for at least $t_{RST} = 2048/f_S$; it resets the device places it in the power-down state, which is the lowest-power dissipation state in the PCM3060.

When \overline{RST} transitions from HIGH to LOW while SCKIx, BCKx, and LRCKx are synchronized, V_{OUTL} and V_{OUTR} are forced to the V_{COM} ($= 0.5 V_{CC}$) level after the fade-out sequence lasting $t_{DACDLY2} = 1616/f_S$, and DOUT is forced to ZERO after $t_{ADCDLY2} = 1936/f_S$ fade-out sequence. After that, the internal reset becomes LOW, the PCM3060 resets and enters into the power-down state, finally all registers and memory except mode control registers are reset. To resume into normal operation, changing \overline{RST} to HIGH again is required, and the sequence shown in **Figure 22** is performed. It is possible to halt SCKIx, BCKx and LRCKx during the power-down state, but all clocks must be resumed prior to starting the power-up sequence. The same fade-in/-out sequence of $V_{OUTL/R}$ and DOUT can be obtained by setting the ADPSV and DAPSV bits through serial mode control port.

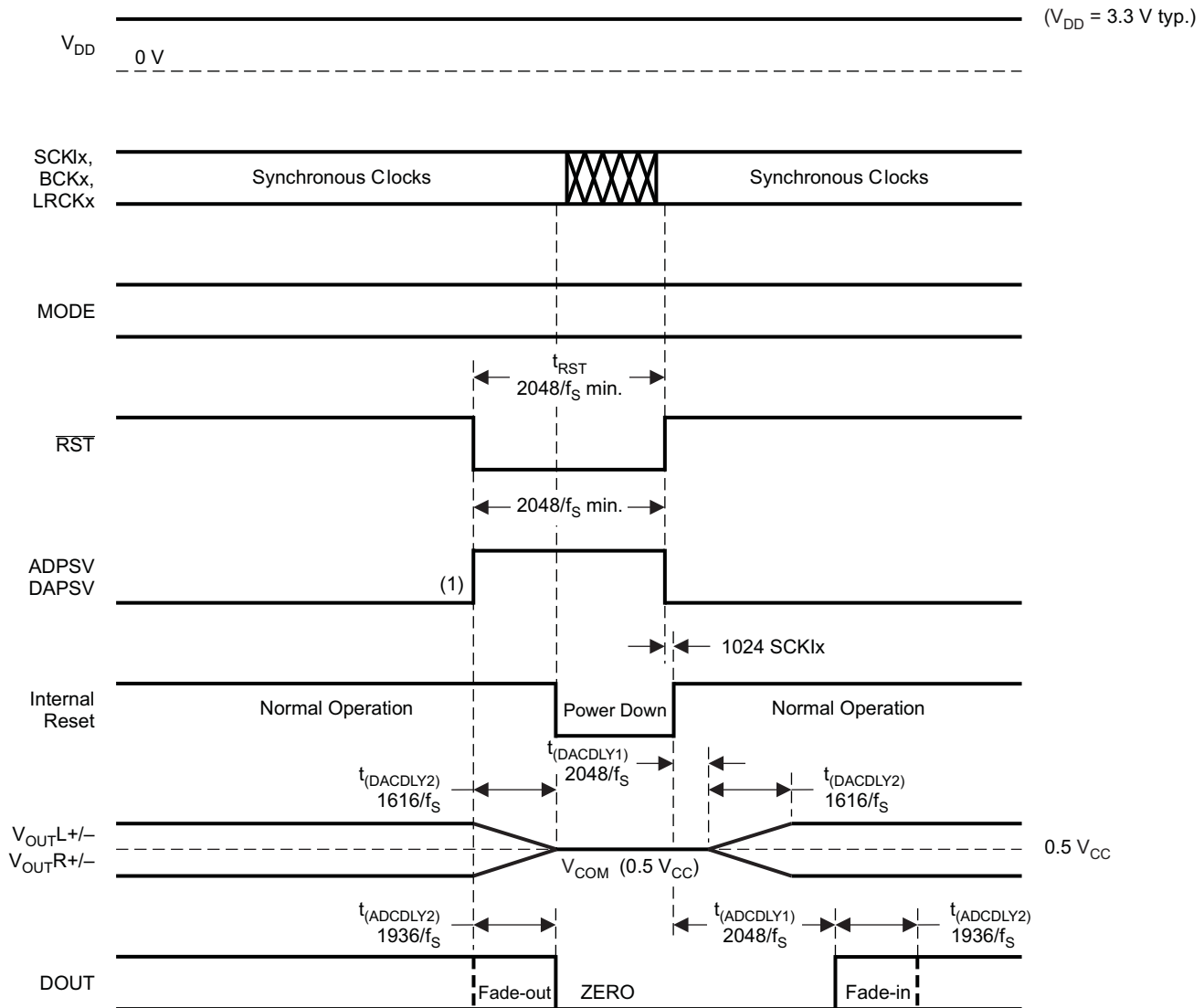
POWER-ON RESET AND EXTERNAL RESET SEQUENCE (Continued)



T0097-02

NOTE: Release from the power-save mode is required if the software control mode is selected.

Figure 22. DAC Output and ADC Output for Power-On Reset



T0098-02

(1) ADPSV and DAPSV control V_{OUTL/R} and DOUT, respectively, with fade-in/out the same as for \overline{RST} .

Figure 23. DAC Output and ADC Output for External Reset

PCM AUDIO INTERFACE

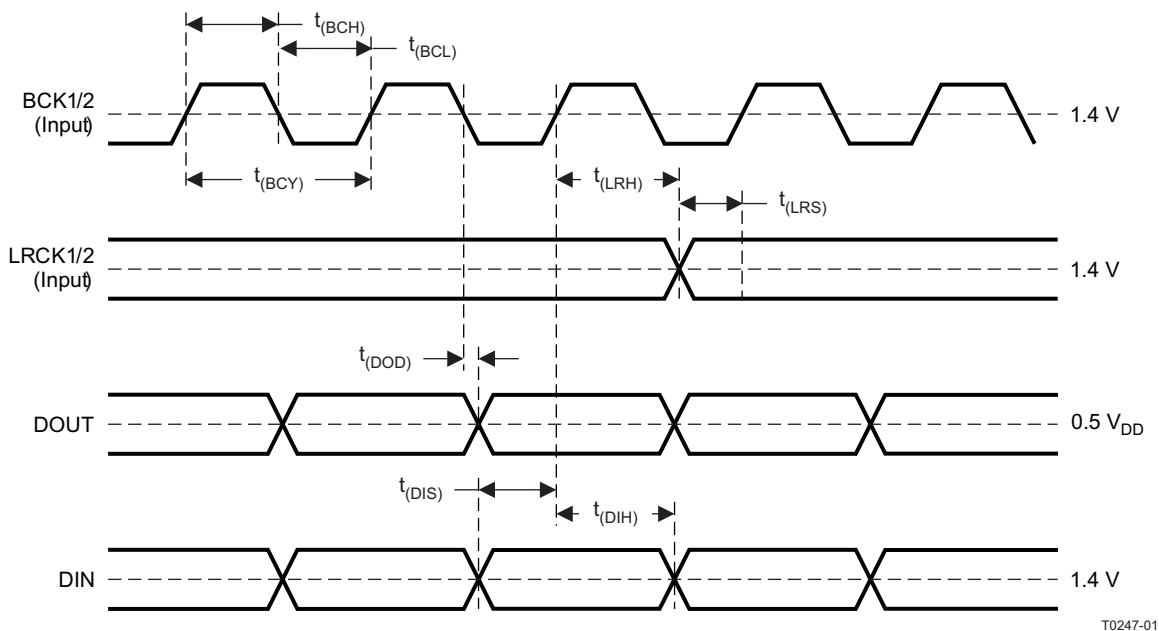
Audio Interface Mode and Timing

The digital audio data can be interfaced in either slave or master mode, and this interface mode is selectable using the serial mode control described in the Mode Control section.

The interface mode is also selectable independently for the ADC and the DAC. DIN is always input to the PCM3060 and DOUT is always an output from the PCM3060. Slave mode is the default mode for both the ADC and the DAC.

In slave mode, BCK1/2 and LRCK1/2 are inputs to the PCM3060, and BCK1/2 must be either $64 f_s$ or $48 f_s$. DIN is sampled on the rising edge of BCK2, and DOUT is changed on the falling edge of BCK1. The default timing specification is shown in Figure 24.

In master mode, BCK1/2 and LRCK1/2 are outputs from the PCM3060. BCK1/2 and LRCK1/2 are generated by the PCM3060 from SCK11/2, and BCK1/2 is fixed at $64 f_s$. DIN is sampled on the rising edge of BCK2, and DOUT is changed on the falling edge of BCK1. The detailed timing specification is shown in Figure 25.

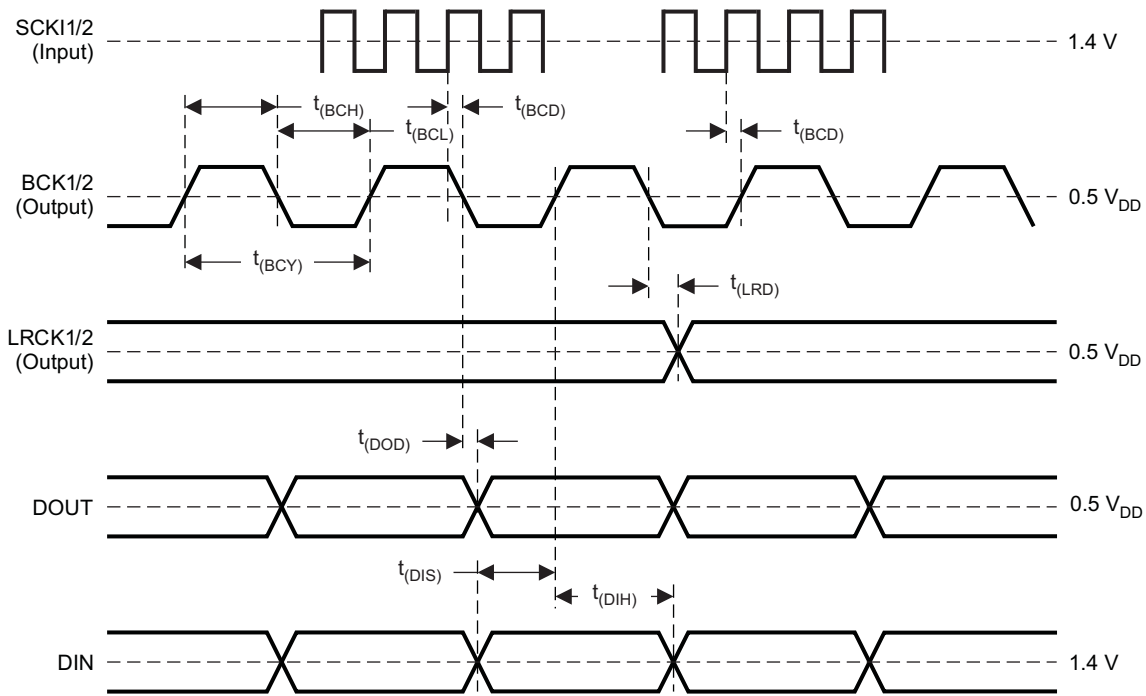


T0247-01

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------------|---|-----|-----|-----|------|
| $t_{(BCY)}$ | BCK1/2 cycle time | 75 | | | ns |
| $t_w(BCH)$ | BCK1/2 high time | 35 | | | ns |
| $t_w(BCL)$ | BCK1/2 low time | 35 | | | ns |
| $t_{(LRS)}$ | LRCK1/2 set-up time to BCK1/2 rising edge | 10 | | | ns |
| $t_{(LRH)}$ | LRCK1/2 hold time to BCK1/2 rising edge | 10 | | | ns |
| $t_{(DIS)}$ | DIN setup time to BCK1/2 rising edge | 10 | | | ns |
| $t_{(DIH)}$ | DIN hold time to BCK1/2 rising edge | 10 | | | ns |
| $t_{(DOD)}$ | DOUT delay time from BCK1/2 falling edge | 15 | | 70 | ns |

NOTE: Load capacitance of output is 20 pF.

Figure 24. Audio Data Interface Timing (Slave Mode: BCK1/2 and LRCK1/2 Work as Inputs)



T0248-01

| SYMBOL | PARAMETERS | MIN | TYP | MAX | UNIT |
|--------------|--|-----------------|-----------------|-----------------|------|
| $t_{(BCY)}$ | BCK1/2 cycle time | $1/64 f_S$ | | | |
| $t_{w(BCH)}$ | BCK1/2 high time | $0.4 t_{(BCY)}$ | $0.5 t_{(BCY)}$ | $0.6 t_{(BCY)}$ | |
| $t_{w(BCL)}$ | BCK1/2 low time | $0.4 t_{(BCY)}$ | $0.5 t_{(BCY)}$ | $0.6 t_{(BCY)}$ | |
| $t_{(LRD)}$ | LRCK1/2 delay time from BCK1/2 falling edge | 0 | | 30 | ns |
| $t_{(DIS)}$ | DIN setup time to BCK1/2 rising edge | 10 | | | ns |
| $t_{(DIH)}$ | DIN hold time to BCK1/2 rising edge | 10 | | | ns |
| $t_{(DOD)}$ | DOUT delay time from BCK1/2 falling edge | 0 | | 30 | ns |
| $t_{(BCD)}$ | BCK1/2 delay time from SCK1/2 rising edge ⁽¹⁾ | 10 | | 40 | ns |

NOTE: Load capacitance of output is 20 pF.

(1) This specification applies for SCK1/2 when the frequency is less than 25 MHz.

Figure 25. Audio Data Interface Timing (Master Mode: BCK1/2 and LRCK1/2 work as Outputs)**Audio Interface Format**

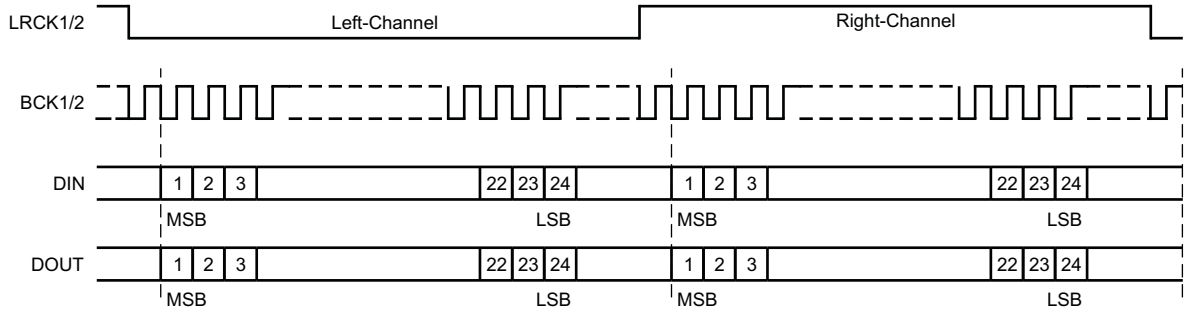
The PCM3060 supports the following four interface formats in both slave and master modes, and they are selectable independently for the ADC and DAC using serial mode control.

- 24-bit I²S format
- 24-bit left-justified format
- 24-bit right-justified format
- 16-bit right-justified format

All formats are provided in MSB-first, 2s complement data format.

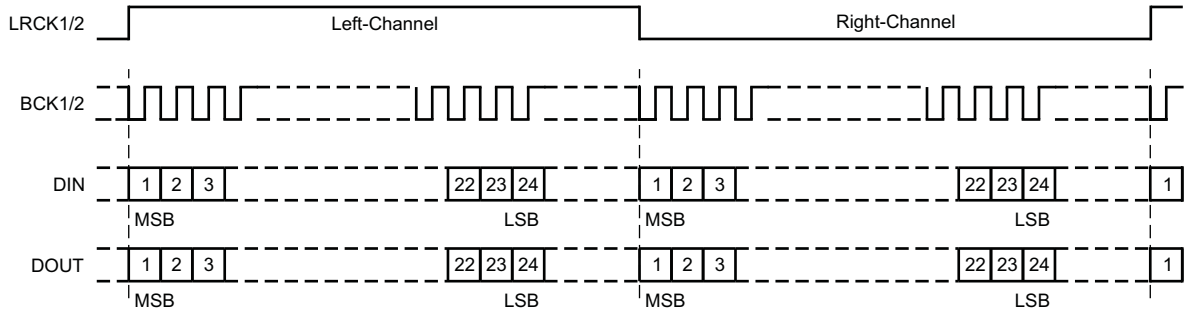
FMT1/2[1:0] = 00

24-Bit, MSB-First, I²S



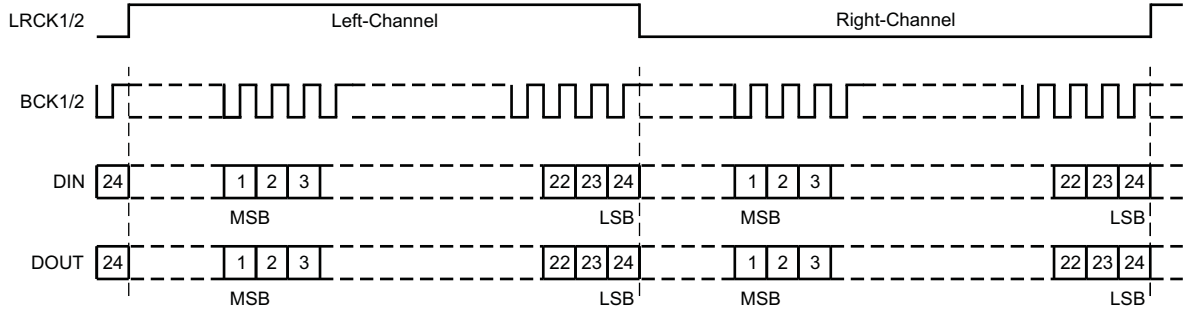
FMT1/2[1:0] = 01

24-Bit, MSB-First, Left-Justified



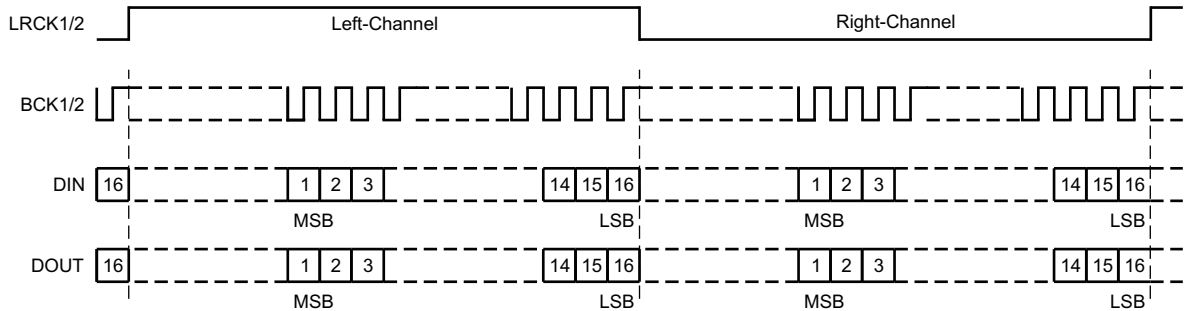
FMT1/2[1:0] = 10

24-Bit, MSB-First, Right-Justified



FMT1/2[1:0] = 11

16-Bit, MSB-First, Right-Justified



T0016-18

Figure 26. Audio Data Input/Output Format

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

As the PCM3060 operates under the system clock (SCK1/2) and the audio sampling clock (LRCK1/2), SCK1/2 and LRCK1/2 must have a specific relationship in slave mode. The PCM3060 does not need a specific phase relationship between audio the interface clocks (LRCK1/2, BCK1/2) and system clock (SCK1/2), but does require a frequency synchronization of LRCK1/2, BCK1/2, and SCK1/2.

If the relationship between SCK12 and LRCK2 changes more than ± 6 BCK2s ($BCK2 = 64 f_s$) or ± 5 BCK2s ($BCK2 = 48 f_s$) due to jitter or frequency change, etc., internal operation of DAC halts within $2/f_s$, and analog output is forced to V_{COM} ($0.5V_{CC}$) until resynchronization of SCK12 to LRCK2 and BCK2 is completed and then $t_{DACDLY3}$ passes by.

If the relationship between SCK11 and LRCK1 changes more than ± 6 BCK1s ($BCK1 = 64 f_s$) or ± 5 BCK1s ($BCK1 = 48 f_s$) due to jitter, frequency change, etc., internal operation of ADC halts within $2/f_s$, and digital output is forced into ZERO code until resynchronization of SCK11 to LRCK1 and BCK1 is completed and then $t_{ADC DLY3}$ passes by.

In case of changes less than ± 5 BCK1/2s ($BCK1/2 = 64$) or ± 4 BCK1/2s ($BCK1/2 = 48$), resynchronization does not occur, and previously described analog/digital output control and discontinuity do not occur.

Figure 27 illustrates the DAC analog output and ADC digital output for loss of synchronization.

During undefined data, it may generate some noise in audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal creates a discontinuity in the data on the analog and digital outputs, which may generate some noise in the audio signal.

The ADC output, DOUT and DAC outputs, and V_{OUTX} hold the previous state if the system clock halts.

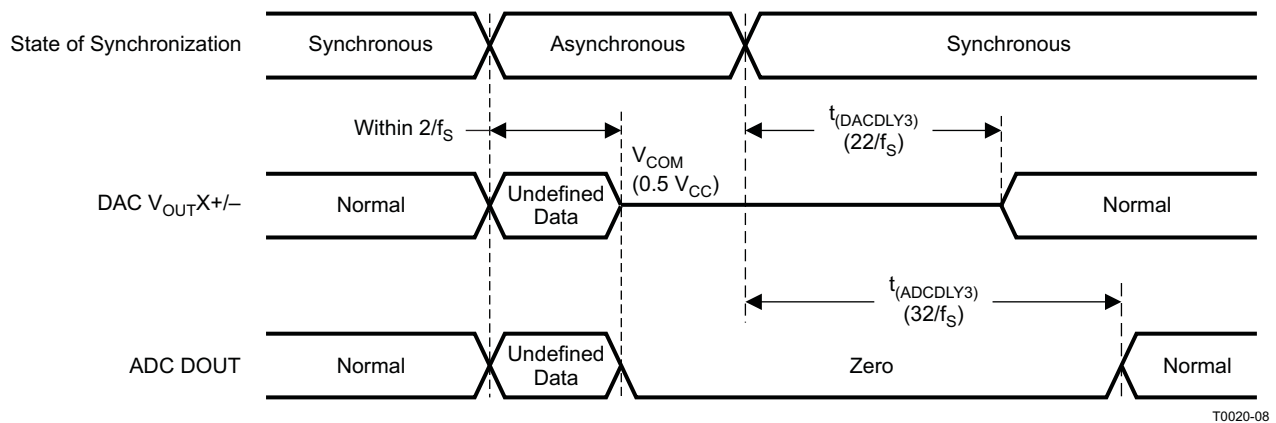


Figure 27. DAC Output and ADC Output for Loss of Synchronization

ANALOG INPUTS TO ADC

The PCM3060 has two independent input channels, V_{INL} and V_{INR} . These are single-ended (unbalanced) inputs, each capable of $0.6 \cdot V_{CC}$ Vpp input with 10-k Ω input resistance, typically.

ANALOG OUTPUTS FROM DAC

The PCM3060 has two independent output channels, V_{OUTL} and V_{OUTR} . These are differential, (balanced) outputs, each capable of driving $0.8 \cdot V_{CC}$ Vpp (1.6-Vpp in differential) typical with a 10-k Ω dc-coupled load. The internal output amplifiers for V_{OUTL+} , V_{OUTL-} and V_{OUTR+} , V_{OUTR-} are biased to V_{COM} , described as follows.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM3060 delta-sigma modulators. The frequency response of this filter is shown in the typical performance curves. This filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications in general. An external low-pass filter is used if further out-of-band noise rejection is required.

V_{OUTX+} , V_{OUTX-} configuration can be changed to single-ended (unbalanced) output via a MODE pin setting or serial mode control, and V_{OUTX+} is assigned as an output pin in single-ended mode.

V_{COM} OUTPUT

One unbuffered common voltage output pin, VCOM (pin 20) is brought out for decoupling purposes. This pin is internally biased to a dc voltage level of $0.5 V_{CC}$ nominal, and is used as an internal common voltage and reference voltage for the ADC and DAC. This pin can be used to bias an external circuit, but the load impedance must be high enough for operation with the output resistance of this pin, which is 12.5 k Ω , typically.

OVERSAMPLING RATE CONTROL

The oversampling rate of ADC of PCM3060 is fixed at $64 f_S$, but the oversampling rate of DAC of PCM3060 is one of $64 f_S$, $32 f_S$ or $16 f_S$, and this is automatically selected by the ratio of system clock frequency and sampling frequency. And it can be also set to double rate, i.e., one of $128 f_S$, $64 f_S$ or $32 f_S$, through serial control.

ZERO FLAGS

Zero-Detect Condition

For each DAC channel, the PCM3060 has a zero-detect circuit that recognizes zero detection when 1024 consecutive zeros have been sampled on DIN.

Zero-Flag Outputs

There are two zero-flag outputs, ZEROL and ZEROR. These pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, etc. These pins can be programmed in following two modes using the serial control port as described in the MODE CONTROL section.

| AZRO | DESCRIPTION | |
|-------------|------------------------------|------------------------------|
| | ZEROL | ZEROR |
| 0 (default) | L-ch zero detection | R-ch zero detection |
| 1 | L-ch and R-ch zero detection | L-ch and R-ch zero detection |

For zero detection, these pins are set to HIGH (1) by default, but the polarity of the zero-flag outputs can be inverted through the serial control port.

| ZREV | DESCRIPTION |
|-------------|-------------------------|
| 0 (default) | HIGH for zero detection |
| 1 | LOW for zero detection |

MODE CONTROL

The PCM3060 supports the following three types of mode control interface and four types of operation configuration, according to the input state of MODE (pin 28) as follows. The pullup or pulldown resistor must be 220 k Ω \pm 5%.

| MODE | MODE CONTROL INTERFACE |
|------------------------------------|--|
| Tie to DGND | 2-wire (I ² C) serial control, selectable V _{OUTX} configuration |
| Pulldown resistor to DGND | 3-wire parallel control, differential V _{OUTX} |
| Pullup resistor to V _{DD} | 3-wire parallel control, single-ended V _{OUTX} |
| Tie to V _{DD} | 3-wire (SPI) serial control, selectable V _{OUTX} configuration |

The input state of the MODE pin is sampled during power-on reset or external reset; therefore, an input change after reset is ignored until the next reset is performed.

The definitions (assignments) of the following three pins are changed by this control mode setting.

| PIN | DEFINITION | | |
|-----|-----------------|------------------|------|
| | SPI | I ² C | H/W |
| 2 | MD | SDA | DEMP |
| 1 | MC | SCL | FMT |
| 27 | \overline{MS} | ADR | IFMD |

In serial mode control, the actual mode control is performed by register write (and read) through an SPI- or I²C-compatible serial control port.

In parallel mode control, three specific functions are controlled directly through high/low settings of three specific pins.

PARALLEL HARDWARE CONTROL

| IFMD (Interface Mode) | DESCRIPTION |
|-----------------------|---|
| LOW | Slave mode for ADC, slave mode for DAC |
| HIGH | Master (256 f _s) mode for ADC, slave mode for DAC |

The audio interface of the ADC and DAC can be independent from each other, but mode selection is applied on both.

| FMT (Interface Format) | DESCRIPTION |
|------------------------|---|
| LOW | 24-bit I ² S for ADC and DAC |
| HIGH | 24-bit left-justified for ADC and DAC |

The audio interface of the ADC and DAC can be independent from each other, but format selection is applied on both.

| DEMP (De-emphasis) | DESCRIPTION |
|--------------------|-------------------------------|
| LOW | De-emphasis off |
| HIGH | De-emphasis on ⁽¹⁾ |

(1) The 44.1-kHz de-emphasis filter is always selected.

3-WIRE (SPI) SERIAL CONTROL

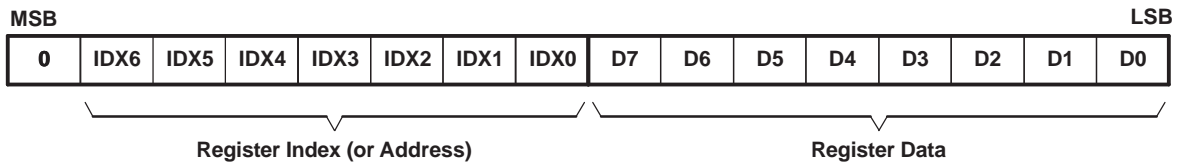
The PCM3060 supports SPI-compatible serial ports, which operate asynchronously to the audio serial interface. The control interface consists of MD, MC, and \overline{MS} . MD is the serial data input, used to program the mode control registers. MC is the serial bit clock, used to shift the data into the control port. \overline{MS} is the select input, used to enable the mode control port.

Register Write Operation

All single-write operations via the serial control port use 16-bit data words. Figure 28 shows the control data word format. The most significant bit must be a 0. There are seven bits, labeled $IDX[6:0]$, that set the register index (address) for the write operation. The least significant eight bits, $D[7:0]$, contain the data to be written to the register specified by $IDX[6:0]$.

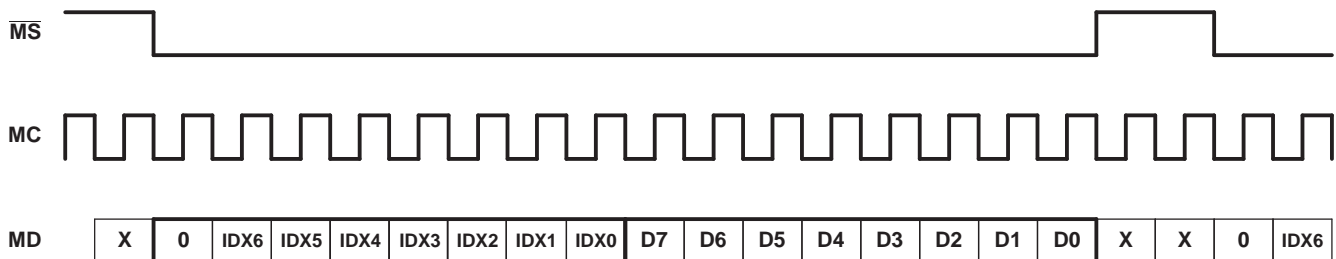
Figure 29 shows the functional timing diagram for single-write operations on the serial control port. \overline{MS} is held in the High state until a register is to be written. To start the register write cycle, \overline{MS} is set to the Low state. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, \overline{MS} is set to High to latch the data into the indexed mode control register.

The PCM3060 supports the multiple-write operation in addition to the single-write operation. Multiple write is performed by sending N-sets of 8-bit register data after the first 16 bits of register address and register data, while keeping the MC clock and \overline{MS} in the Low state. Closing the multiple-write operation is done by setting \overline{MS} to the High state.



R0001-01

Figure 28. Control Data Word Format for MD

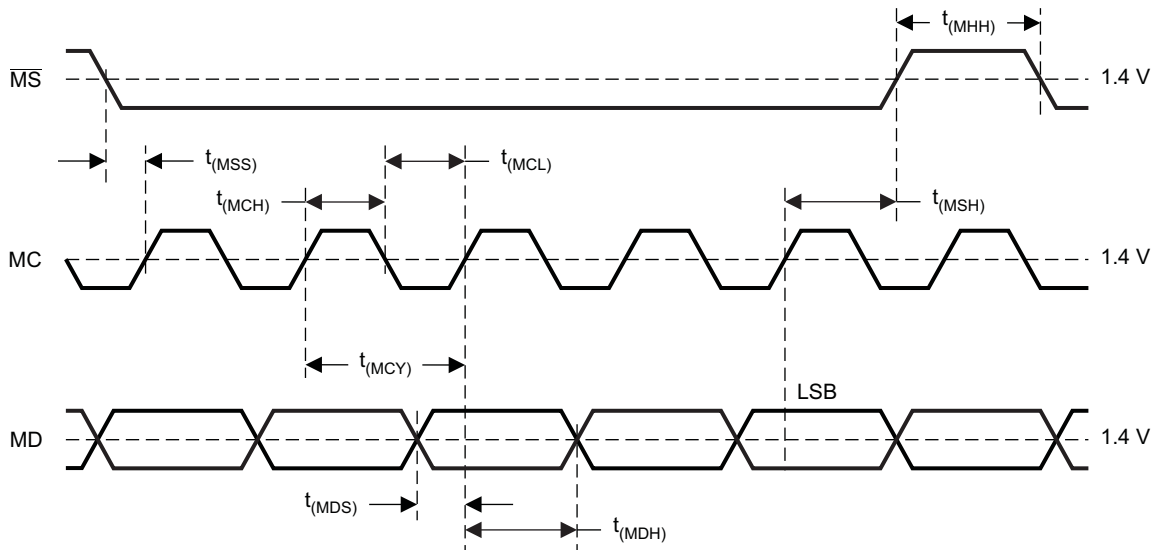


T0048-01

Figure 29. Register Write Operation

Timing Requirements

Figure 30 shows a detailed timing diagram for the 3-wire serial control interface. These timing parameters are critical for proper control port operation.



T0013-10

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------------|--|-------------|-----|------|
| $t_{(MCY)}$ | MC cycle time | 100 | | ns |
| $t_{w(MCL)}$ | MC low-level time | 40 | | ns |
| $t_{w(MCH)}$ | MC high-level time | 40 | | ns |
| $t_{(MHH)}$ | \overline{MS} high-level time | $t_{(MCY)}$ | | ns |
| $t_{(MSS)}$ | \overline{MS} falling edge to MC rising edge | 15 | | ns |
| $t_{(MSH)}$ | \overline{MS} rising edge from MC rising edge for LSB ⁽¹⁾ | 15 | | ns |
| $t_{(MDH)}$ | MD hold time | 15 | | ns |
| $t_{(MDS)}$ | MD setup time | 15 | | ns |

(1) MC rise edge for LSB to \overline{MS} rise edge.

Figure 30. Control Interface Timing for SPI

TWO-WIRE (I²C) SERIAL CONTROL

The PCM3060 supports the I²C-compatible serial bus and the data transmission protocol for standard-mode and fast-mode (C_B max = 100 pF) as a slave device. This protocol is explained in the well-known I²C 2.0 specification.

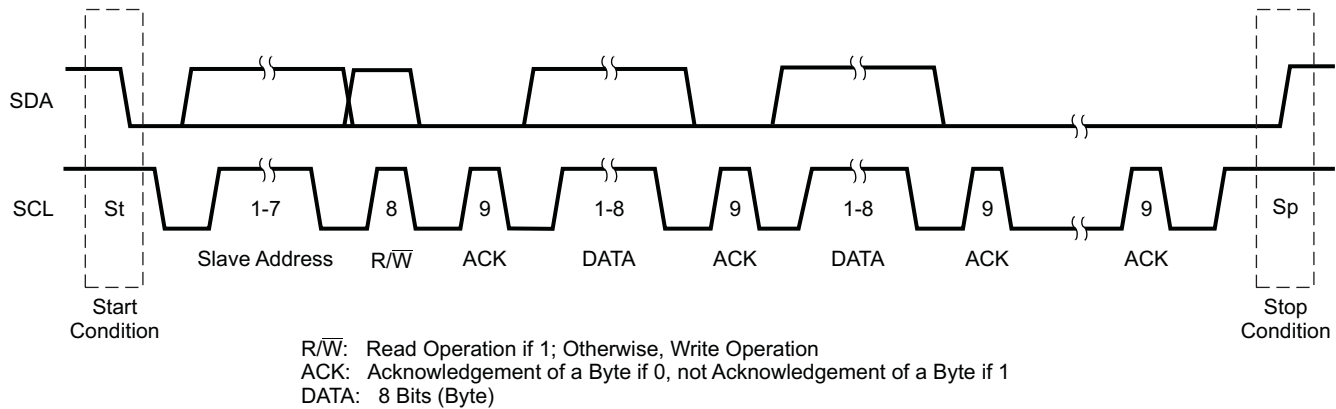
Slave Address

| MSB | | | | | | LSB | |
|-----|---|---|---|---|---|-----|-----|
| 1 | 0 | 0 | 0 | 1 | 1 | ADR | R/W |

The PCM3060 has 7 bits for its own slave address. The first six bits (MSBs) of the slave address are factory preset to 10 0011. The next bit of the address byte is the device select bit, which can be user-defined by the ADR pin (pin 27). Two PCM3060s at maximum can be connected on the same bus at one time. Each PCM3060 responds when it receives its own slave address.

Packet Protocol

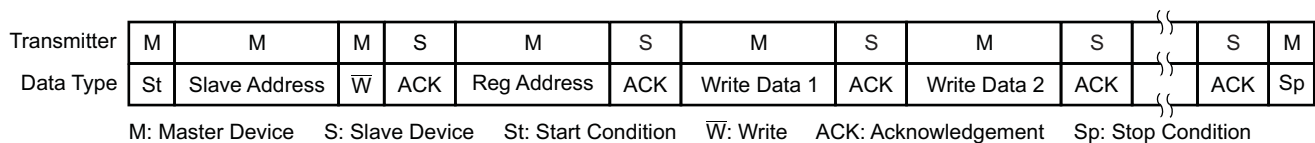
A master device must control packet protocol, which consists of a start condition, slave address with read/write bit, data if write or acknowledgment if read, and stop condition. The PCM3060 supports the slave receiver function.



T0049-06

Write Operation

The PCM3060 supports the receiver function. A master can write to any PCM3060 registers using single or multiple accesses. The master sends a PCM3060 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by 1 automatically. When the index register reaches 4Ah, the next value is 40h. When undefined registers are accessed, the PCM3060 does not send an acknowledgment. Figure 31 is a diagram of the write operation. The register address and the write data are 8-bit in MSB-first format.

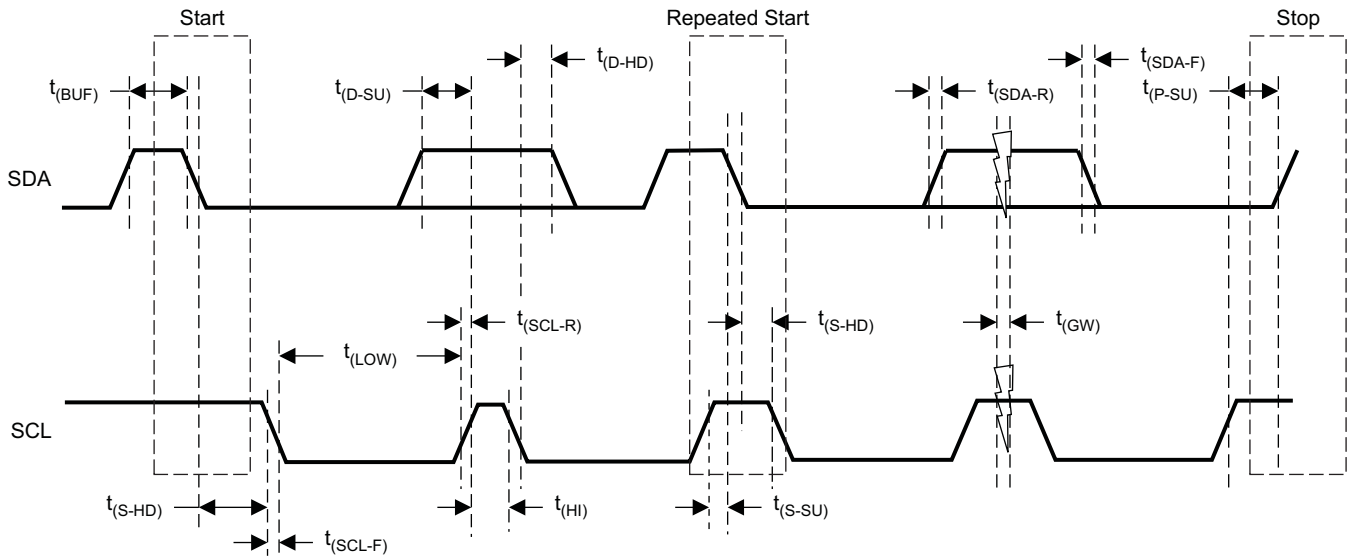


R0002-04

Figure 31. Framework for Write Operation

Timing Diagram

The detailed timing diagram for SCL and SDA is shown as follows.



T0050-04

Timing Characteristics

| SYMBOL | PARAMETER | STANDARD MODE | | FAST MODE | | UNIT |
|---------------|---|---------------|------|----------------|-----|---------|
| | | MIN | MAX | MIN | MAX | |
| $f_{(SCL)}$ | SCL clock frequency | | 100 | | 400 | kHz |
| $t_{(BUF)}$ | Bus free time between STOP and START conditions | 4.7 | | 1.3 | | μ s |
| $t_{(LOW)}$ | Low period of the SCL clock | 4.7 | | 1.3 | | μ s |
| $t_{(HI)}$ | High period of the SCL clock | 4 | | 0.6 | | μ s |
| $t_{(S-SU)}$ | Setup time for START/repeated START condition | 4.7 | | 0.6 | | μ s |
| $t_{(S-HD)}$ | Hold time for START/repeated START condition | 4 | | 0.6 | | μ s |
| $t_{(D-SU)}$ | Data setup time | 250 | | 100 | | ns |
| $t_{(D-HD)}$ | Data hold time | 0 | 3450 | 0 | 900 | ns |
| $t_{(SCL-R)}$ | Rise time of SCL signal | | 1000 | $20 + 0.1 C_B$ | 300 | ns |
| $t_{(SCL-F)}$ | Fall time of SCL signal | | 1000 | $20 + 0.1 C_B$ | 300 | ns |
| $t_{(SDA-R)}$ | Rise time of SDA signal | | 1000 | $20 + 0.1 C_B$ | 300 | ns |
| $t_{(SDA-F)}$ | Fall time of SDA signal | | 1000 | $20 + 0.1 C_B$ | 300 | ns |
| $t_{(P-SU)}$ | Setup time for STOP condition | 4 | | 0.6 | | μ s |
| $t_{(GW)}$ | Allowable glitch width | | N/A | | 50 | ns |
| C_B | Capacitive load for SDA and SCL lines | | 400 | | 100 | pF |
| | Noise margin at high level for each connected device (including hysteresis) | $0.2 V_{DD}$ | | $0.2 V_{DD}$ | | V |
| | Noise margin at low level for each connected device (including hysteresis) | $0.1 V_{DD}$ | | $0.1 V_{DD}$ | | V |
| | Hysteresis of Schmitt-trigger input | N/A | | $0.05 V_{DD}$ | | V |

Figure 32. Control Interface Timing for I²C

MODE CONTROL REGISTERS

The PCM3060 has many user-programmable functions which are accessed via control registers, and they are programmed through the SPI or I²C serial control port. Table 3 lists the available mode control functions along with reset default conditions and associated register addresses. The register map is shown in Table 3.

Table 3. User-Programmable Mode Control Functions

| FUNCTION RESET | DEFAULT | REGISTER | LABEL |
|---|------------------------------|-----------|----------------------|
| Mode control register reset (ADC and DAC) | Normal operation | 64 | MRST |
| System reset (ADC and DAC) | Normal operation | 64 | SRST |
| ADC power-save control (ADC) | Power save | 64 | ADPSV |
| DAC power-save control (DAC) | Power save | 64 | DAPSV |
| VOOUT configuration control (DAC) | Differential | 64 | S/E |
| Digital attenuation control, 0 dB to –100 dB in 0.5-dB steps (DAC) | 0 dB, no attenuation | 65 and 66 | AT21[7:0], AT22[7:0] |
| Clock select for DAC operation (DAC) | CLK2 enable | 67 | CSEL2 |
| Master/slave mode for DAC audio interface (DAC) | Slave | 67 | M/S 2[2:0] |
| Interface format for DAC audio interface (DAC) | I ² S | 67 | FMT2[1:0] |
| Oversampling rate control (DAC) | Low (x64/x32/x16) | 68 | OVER |
| Output phase select (DAC) | Normal | 68 | DREV2 |
| Soft-mute control (DAC) | Mute disabled | 68 | MUT22, MUT21 |
| Digital filter rolloff control (DAC) | Sharp rolloff | 69 | FLT |
| De-emphasis sampling rate selection (DAC) | 44.1 kHz | 69 | DMF[1:0] |
| De-emphasis function control (DAC) | De-emphasis disabled | 69 | DMC |
| Zero-flag polarity control (DAC) | High for detection | 69 | ZREV |
| Zero-flag form select (DAC) | L-ch, R-ch independent | 69 | AZRO |
| Digital attenuation control, 20 dB to –100 dB in 0.5-dB steps (ADC) | 0 dB, no attenuation | 70 and 71 | AT11[7:0], AT12[7:0] |
| Clock select for ADC operation (ADC) | CLK1 enable | 72 | CSEL1 |
| Master/slave mode for ADC audio interface (ADC) | Slave | 72 | M/S1[2:0] |
| Interface format for ADC audio interface (ADC) | I ² S | 72 | FMT1[1:0] |
| Zero-cross detection disable for digital attenuation control (ADC) | Zero-cross detection enabled | 73 | ZCDD |
| HPF bypass control (ADC) | Bypass disabled | 73 | BYP |
| Input phase select (ADC) | Normal | 73 | DREV1 |
| Soft-mute control (ADC) | Mute disabled | 73 | MUT12, MUT11 |

Table 4. Register Map

| REGISTER ADDRESS | | | | | | | | | | DATA | | | | | | | |
|------------------|-------------|-----|-----|-----|-----|-----|-----|----|----|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-------|
| HEX | DEC | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 40h | Register 64 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | MRST | SRST | ADPSV | DAPSV | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | S/E |
| 41h | Register 65 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | AT217 | AT216 | AT215 | AT214 | AT213 | AT212 | AT211 | AT210 |
| 42h | Register 66 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | AT227 | AT226 | AT225 | AT224 | AT223 | AT222 | AT221 | AT220 |
| 43h | Register 67 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | CSEL2 | M/S 22 | M/S 21 | M/S 20 | RSV ⁽¹⁾ | RSV ⁽¹⁾ | FMT21 | FMT20 |
| 44h | Register 68 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | RSV ⁽¹⁾ | OVER | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | DREV2 | MUT22 | MUT21 |
| 45h | Register 69 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | FLT | DMF1 | DMF0 | DMC | RSV ⁽¹⁾ | RSV ⁽¹⁾ | ZREV | AZRO |
| 46h | Register 70 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | AT117 | AT116 | AT115 | AT114 | AT113 | AT112 | AT111 | AT110 |
| 47h | Register 71 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | AT127 | AT126 | AT125 | AT124 | AT123 | AT122 | AT121 | AT120 |
| 48h | Register 72 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | CSEL1 | M/S 12 | M/S 11 | M/S 10 | RSV ⁽¹⁾ | RSV ⁽¹⁾ | FMT11 | FMT10 |
| 49h | Register 73 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | ZCDD | BYP | DREV1 | MUT12 | MUT11 |

(1) RSV means reserved for factory use or future extension, and these bits should be set to 0 during regular operation. Do not write any values in addresses other than those listed.

REGISTER DEFINITIONS

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
|-------------|-----|-----|-----|-----|-----|-----|----|----|----|------|------|-------|-------|-----|-----|-----|-----|
| Register 64 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MRST | SRST | ADPSV | DAPSV | RSV | RSV | RSV | S/E |

MRST: Mode Control Register Reset (ADC and DAC)

Default value: 1

| | |
|----------|----------------------------|
| MRST = 0 | Set default value |
| MRST = 1 | Normal operation (default) |

The MRST bit controls reset of the mode control registers to their default values. Pop noise may be generated. Returning the MRST bit to 1 is not required, as the MRST bit is automatically set to 1 after a mode control register reset.

SRST: System Reset (ADC and DAC)

Default value: 1

| | |
|----------|----------------------------|
| SRST = 0 | Resynchronization |
| SRST = 1 | Normal operation (default) |

The SRST bit controls system reset, the relation between system clock and sampling clock is re-synchronized, and ADC operation and DAC operation is restarted. The mode control register is not reset and the PCM3060 does not go into power down state, but pop-noise may be generated. Returning the SRST bit to 1 is not required, as the SRST bit is automatically set to 1 after triggering a system reset.

ADPSV: ADC Power-Save Control (ADC)

Default value: 1

| | |
|-----------|---------------------------|
| ADPSV = 0 | Normal operation |
| ADPSV = 1 | Power-save mode (default) |

The ADPSV bit controls the ADC power-save mode. In power-save mode, DOUT is forced to ZERO with a fade-out sequence, the internal ADC data are reset, and the ADC goes into the power-down state. For power-save mode release, a fade-in sequence is applied on DOUT during the resume process. The serial mode control is enabled during this mode. A waiting time of more than $2048/f_s$ is required for the proper status change by this power save control on/off. As the default state after power on is the power-save mode and DOUT is disabled (ZERO), release from the power-save mode is required for normal operation. The detailed sequence and timing for ADPSV control is shown [Figure 22](#) and [Figure 23](#).

NOTE:

It is recommended that changing/stopping clocks or changing the audio interface mode be performed in power-down mode in order to avoid unexpected pop/click noise and performance degradation.

DAPSV: DAC Power-Save Control (DAC)

Default value: 1

| | |
|-----------|---------------------------|
| DAPSV = 0 | Normal operation |
| DAPSV = 1 | Power-save mode (default) |

The DAPSV bit controls DAC power-save mode. In power-save mode, DAC outputs are forced to V_{com} with a fade-out sequence, the internal DAC data are reset and the DAC goes into the power-down state. For power-save mode release, a fade-in sequence is applied on the DAC outputs in resume process. The serial mode control is enabled during this mode. A waiting time of more than $2048/f_S$ is required for the proper status change by this power-save control on/off. As the default state after power on is the power-save mode and the DAC outputs are disabled (V_{COM}), release from the power-save mode is required for normal operation. The detailed sequence and timing for DAPSV control is shown [Figure 22](#) and [Figure 23](#).

NOTE:

It is recommended that changing/stopping clocks or changing the audio interface mode be performed in power-down mode in order to avoid unexpected pop/click noise and performance degradation.

S/E: DAC Output Configuration Control (DAC)

Default value: 0

| | |
|---------|------------------------|
| S/E = 0 | Differential (default) |
| S/E = 1 | Single-ended |

The S/E bit allows the user to select the configuration of the DAC output on the V_{OUTX} pins according to application circuit.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-------|-------|-------|-------|-------|-------|-------|-------|
| Register 65 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | AT217 | AT216 | AT215 | AT214 | AT213 | AT212 | AT211 | AT210 |
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 66 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | AT227 | AT226 | AT225 | AT224 | AT223 | AT222 | AT221 | AT220 |

AT2x[7:0]: Digital Attenuation Level Setting (DAC)

Where $x = 1$ or 2 , corresponding to the DAC output V_{OUTL} ($x = 1$) and V_{OUTR} ($x = 2$).

Default value: 1111 1111b

| AT2x[7:0] | DECIMAL VALUE | ATTENUATION LEVEL SETTING |
|------------|---------------|--------------------------------|
| 1111 1111b | 255 | 0 dB, no attenuation (default) |
| 1111 1110b | 254 | –0.5 dB |
| 1111 1101b | 253 | –1 dB |
| : | : | : |
| 1000 0001b | 129 | –63 dB |
| 1000 0000b | 128 | –63.5 dB |
| 0111 1111b | 127 | –64 dB |
| : | : | : |
| 0011 1000b | 56 | –99.5 dB |
| 0011 0111b | 55 | –100 dB |
| 0011 0110b | 54 | Mute |
| : | : | : |
| 0000 0000b | 0 | Mute |

Each DAC channel (V_{OUTL} and V_{OUTR}) has a digital attenuator function. The attenuation level may be set from 0 dB to –100 dB in 0.5-dB steps, and also may be set to infinite attenuation (mute). The attenuation level change from current value to target value is performed by incrementing or decrementing one 0.5-dB step for every $8/f_s$ time interval. While the attenuation level change sequence is in progress, new commands for attenuation level change are not processed, but the new command overwrites the previous command in the command buffer. The last command for attenuation level change is performed after the present attenuation level change sequence is finished.

The attenuation level for each channel can be set individually using the following formula, and the foregoing table shows attenuation levels for various settings:

Attenuation level (dB) = $0.5 \times (AT2x[7:0]_{DEC} - 255)$, where $AT2x[7:0]_{DEC} = 0$ through 255 for $AT2x[7:0]_{DEC} = 0$ through 54, the level is set to infinite attenuation (mute).

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-------|--------|--------|--------|-----|-----|-------|-------|
| Register 67 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | CSEL2 | M/S 22 | M/S 21 | M/S 20 | RSV | RSV | FMT21 | FMT20 |

CSEL2: Clock Select for DAC Operation

Default value: 0 (SCKI2, BCK2, LRCK2 enabled for DAC operation)

| | |
|-----------|--|
| CSEL2 = 0 | SCKI2, BCK2, LRCK2 enabled for DAC operation (default) |
| CSEL2 = 1 | SCKI1, BCK1, LRCK1 enabled for DAC operation |

The CSEL2 bit controls system clock and audio interface clocks for the DAC operation.

SCKI2, BCK2, LRCK2 are used for the DAC portion if CSEL2 = 0 (default), and SCKI1, BCK1, LRCK1 are used for DAC operation if CSEL2 = 1.

M/S 2[2:0]: Audio Interface Mode for DAC

Default value: 000 (slave mode)

| M/S 2[2:0] | Audio Interface Mode for DAC |
|------------|---------------------------------|
| 0 0 0 | Slave mode (default) |
| 0 0 1 | Master mode, 768 f _S |
| 0 1 0 | Master mode, 512 f _S |
| 0 1 1 | Master mode, 384 f _S |
| 1 0 0 | Master mode, 256 f _S |
| 1 0 1 | Master mode, 192 f _S |
| 1 1 0 | Master mode, 128 f _S |
| 1 1 1 | Reserved |

The M/S 2[2:0] bits control the audio interface mode for the DAC.

FMT2[1:0]: Audio Interface Format for DAC

Default value: 00 (I²S Mode)

| FMT2[1:0] | Audio Interface Format for DAC |
|-----------|--|
| 0 0 | 24-bit I ² S format (default) |
| 0 1 | 24-bit left-justified format |
| 1 0 | 24-bit right-justified format |
| 1 1 | 16-bit right-justified format |

The FMT2[1:0] bits control the audio interface format for the DAC.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-----|------|-----|-----|-----|-------|-------|-------|
| Register 68 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | RSV | OVER | RSV | RSV | RSV | DREV2 | MUT22 | MUT21 |

OVER: Oversampling Rate Control (DAC)

Default value: 0

| OVER | System clock = 512 f_S or 768 f_S | System clock = 256 f_S or 384 f_S | System clock = 128 f_S or 192 f_S |
|----------|---------------------------------------|---------------------------------------|---------------------------------------|
| OVER = 0 | ×64 Oversampling (default) | ×32 Oversampling (default) | ×16 Oversampling (default) |
| OVER = 1 | ×128 Oversampling | ×64 Oversampling | ×32 Oversampling |

The OVER bit is used to control the oversampling rate of the delta-sigma D/A converters.

Setting OVER = 1 might improve out-of-band noise characteristics in some application environments, but it might also slightly affect baseband performance.

Writing over this bit during normal operation may generate pop noise.

DREV2: Output Phase Select (DAC)

Default value: 0

| | |
|-----------|-------------------------|
| DREV2 = 0 | Normal output (default) |
| DREV2 = 1 | Inverted output |

The DREV2 bit is used to control the phase of the analog signal outputs (V_{OUTL} and V_{OUTR}).

MUT2x: Soft Mute Control (DAC)

where $x = 1$ or 2 , corresponding to the DAC output V_{OUTL} ($x = 1$) and V_{OUTR} ($x = 2$).

Default value: 0

| | |
|-----------|-------------------------|
| MUT2x = 0 | Mute disabled (default) |
| MUT2x = 1 | Mute enabled |

The mute bits, MUT21 and MUT22, are used to enable or disable the soft mute function for the corresponding DAC outputs, V_{OUTL} and V_{OUTR} . The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUT2x = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUT2x = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation at the rate of one 0.5-dB step for every $8/f_S$ time interval. By setting MUT2x = 0, the attenuator is increased to the previously programmed attenuation level at the rate of one 0.5-dB step for every $8/f_S$ time interval. This provides pop-free muting of the DAC output.

| | | | | | | | | | | | | | | | | |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-----|------|------|-----|-----|-----|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 69 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | FLT | DMF1 | DMF0 | DMC | RSV | RSV | ZREV | AZRO |

FLT: Digital Filter Rolloff Control (DAC)

Default value: 0

| | |
|---------|-------------------------|
| FLT = 0 | Sharp rolloff (Default) |
| FLT = 1 | Slow rolloff |

The FLT bit allows the user to select the digital filter roll-off that is best suited to their application. Sharp and Slow filter roll-off selections are available. The filter responses for these selections are shown in the *Typical Performance Curves* section of this data sheet.

DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function (DAC)

Default value: 00

| DMF[1:0] | De-Emphasis Sampling Rate Selection |
|----------|-------------------------------------|
| 0 0 | 44.1 kHz (default) |
| 0 1 | 48 kHz |
| 1 0 | 32 kHz |
| 1 1 | Reserved |

The DMF[1:0] bits are used to select the sampling frequency of the digital de-emphasis function when it is enabled.

DMC: Digital De-Emphasis Function Control (DAC)

Default value: 0

| | |
|---------|--------------------------------|
| DMC = 0 | De-emphasis disabled (default) |
| DMC = 1 | De-emphasis enabled |

The DMC bit is used to enable or disable the digital de-emphasis function. See the plots shown in the *Typical Performance Curves* section of this data sheet for frequency characteristics.

ZREV: Zero-Flag Polarity Select (DAC)

Default value: 0

| | |
|----------|--------------------------------|
| ZREV = 0 | High for zero detect (default) |
| ZREV = 1 | Low for zero detect |

The ZREV bit is used to control the polarity of zero flag pins.

AZRO: Zero-Flag Function Select (DAC)

Default value: 0

| | | |
|----------|--------------------------------------|--------------------------------------|
| AZRO = 0 | ZEROL: L-ch ZERO detection (default) | ZEROR: R-ch ZERO detection (default) |
| AZRO = 1 | ZEROL: L and R ZERO detection | ZEROR: L and R ZERO detection |

The AZRO bit is used to select the function of zero flag pins.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-------|-------|-------|-------|-------|-------|-------|-------|
| Register 70 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | AT117 | AT116 | AT115 | AT114 | AT113 | AT112 | AT111 | AT110 |
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 71 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | AT127 | AT126 | AT125 | AT124 | AT123 | AT122 | AT121 | AT120 |

AT1x[7:0]: Digital Attenuation Level Setting (ADC)

where x = 1 or 2, corresponding to the ADC output L-ch part of DOUT (x = 1) or R-ch part of DOUT (x = 2).

Default value: 1101 0111b

| AT1x[7:0] | DECIMAL VALUE | ATTENUATION LEVEL SETTING |
|------------|---------------|--------------------------------|
| 1111 1111b | 255 | 20 dB |
| 1111 1110b | 254 | 19.5 dB |
| 1111 1101b | 253 | 19 dB |
| : | : | : |
| 1101 1000b | 216 | 0.5 dB |
| 1101 0111b | 215 | 0 dB, no attenuation (default) |
| 1101 0110b | 214 | –0.5 dB |
| : | : | : |
| 0001 0000b | 16 | –99.5 dB |
| 0000 1111b | 15 | –100 dB |
| 0000 1110b | 14 | Mute |
| : | : | : |
| 0000 0000b | 0 | Mute |

Each ADC channel has a digital attenuator function with 20-dB gain. The attenuation level may be set from 20 dB to –100 dB in 0.5-dB steps, and also may be set to infinite attenuation (mute). The attenuation level change from the current value to the target value is performed by incrementing or decrementing one by 0.5-dB step at the timing of zero-cross detection on the input signal which is sampled for every $1/f_S$ time interval, or for every $8/f_S$ time interval if the zero-cross detection mode is disabled by ZCDD setting. If a zero-crossing is not detected for $512/f_S$, actual level change is done for every $1/f_S$ time interval until a zero-crossing is detected again. While the attenuation level change sequence is in progress, new commands for attenuation level change are not processed, but the new command overwrites the previous command in the command buffer. The last command for attenuation level change is performed after the present attenuation level change sequence is finished.

The attenuation level for each channel can be set individually using the following formula, and the above table shows attenuation levels for various settings:

Attenuation level (dB) = $0.5 \times (AT1x[7:0]_{DEC} - 215)$, where $AT1x[7:0]_{DEC} = 0$ through 255 for $AT1x[7:0]_{DEC} = 0$ through 14, the level is set to infinite attenuation (mute).

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
|-------------|-----|-----|-----|-----|-----|-----|----|----|----|-------|--------|--------|--------|-----|-----|-------|-------|
| Register 72 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | CSEL1 | M/S 12 | M/S 11 | M/S 10 | RSV | RSV | FMT11 | FMT10 |

CSEL1: Clock Select for ADC Operation

Default value: 0 (SCK11, BCK1, LRCK1 enabled for ADC operation)

| | |
|-----------|--|
| CSEL1 = 0 | SCK11, BCK1, LRCK1 enabled for ADC operation (default) |
| CSEL1 = 1 | SCKI2, BCK2, LRCK2 enabled for ADC operation |

The CSEL1 bit controls the system clock and audio interface clocks for the ADC operation.

SCK11, BCK1, LRCK1 are used for ADC portion if CSEL1 = 0 (default), and SCKI2, BCK2, LRCK2 are used for ADC portion if CSEL1 = 1.

M/S 1[2:0]: Audio Interface Mode for ADC

Default value: 000 (slave mode)

| M/S 1[2:0] | Audio Interface Mode for ADC |
|------------|---------------------------------|
| 0 0 0 | Slave mode (default) |
| 0 0 1 | Master mode, 768 f _S |
| 0 1 0 | Master mode, 512 f _S |
| 0 1 1 | Master mode, 384 f _S |
| 1 0 0 | Master mode, 256 f _S |
| 1 0 1 | Reserved |
| 1 1 0 | Reserved |
| 1 1 1 | Reserved |

The M/S 1[2:0] bits control the audio interface mode for the ADC.

FMT1[1:0]: Audio Interface Format for ADC

Default value: 00 (I²S mode)

| FMT1[1:0] | Audio Interface Format for ADC |
|-----------|--|
| 0 0 | 24-bit I ² S format (default) |
| 0 1 | 24-bit left-justified format |
| 1 0 | 24-bit right-justified format |
| 1 1 | 16-bit right-justified format |

The FMT1[1:0] bits control the audio interface mode for ADC.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|------|-----|-------|-------|-------|
| Register 73 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | RSV | RSV | RSV | ZCDD | BYP | DREV1 | MUT12 | MUT11 |

ZCDD: Zero-Cross Detection Disable for Digital Attenuation (ADC)

Default value: 0

| | |
|----------|--|
| ZCDD = 0 | Zero-cross detection enabled (default) |
| ZCDD = 1 | Zero-cross detection disabled |

The ZCDD bit controls the zero-cross detect function for digital attenuation and mute. When zero-cross detection is enabled, the actual level change for digital attenuation and mute is done at the timing of zero-cross detection on the input signal which is sampled for every $1/f_S$ time interval. If zero-crossing is not detected for $512/f_S$, the actual level change is done for every $1/f_S$ time interval until a zero-crossing is detected again as timeout control for no zero-crossing input signal. When zero-cross detection is disabled, the actual level change is done at the timing of $8/f_S$ time interval.

BYP: HPF Bypass Control (ADC)

Default value: 0

| | |
|---------|--------------------------------------|
| BYP = 0 | Normal output, HPF enabled (default) |
| BYP = 1 | Bypassed output, HPF disabled |

The BYP bit controls the HPF function; the dc component of the input signal and the internal dc offset are converted in bypass mode.

DREV1: Input Phase Select (ADC)

Default value: 0

| | |
|-----------|------------------------|
| DREV1 = 0 | Normal input (default) |
| DREV1 = 1 | Inverted input |

The DREV1 bit is used to control the phase of analog signal inputs (V_{INL} and V_{INR}).

MUT1x: Soft Mute Control (ADC)

where $x = 1$ or 2 , corresponding to the ADC output L-ch part of DOUT ($x = 1$) and R-ch part of DOUT ($x = 2$).

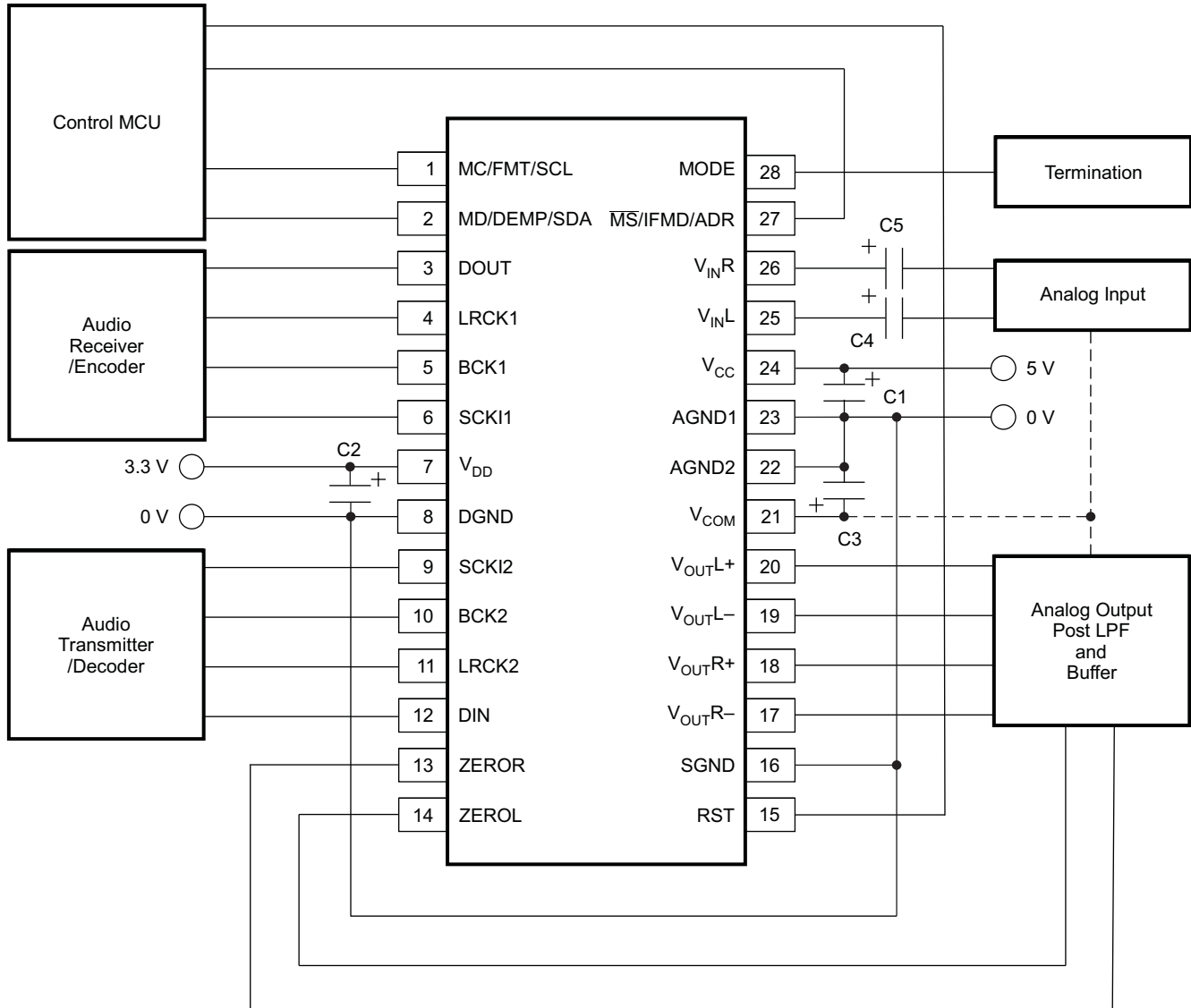
Default value: 0

| | |
|-----------|-------------------------|
| MUT1x = 0 | Mute disabled (default) |
| MUT1x = 1 | Mute enabled |

The mute bits, MUT11 and MUT12, are used to enable or disable the soft mute function for the corresponding ADC outputs, DOUT. The soft mute function is incorporated into the digital attenuators. When mute is disabled ($MUT1x = 0$), the attenuator and ADC operate normally. When mute is enabled by setting $MUT1x = 1$, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation in 0.5 dB step at the timing of zero-cross detection on the input signal which is sampled for every $1/f_S$ time interval, or for every $8/f_S$ time interval if zero-cross detection mode is disabled by ZCDD setting. If a zero-crossing is not detected for $512/f_S$, actual level change is done for every $1/f_S$ time interval until zero-crossing is detected again. By setting $MUT1x = 0$, the attenuator is increased to the previously programmed attenuation level in 0.5 dB step in the same manner as for decreasing. This provides pop-free muting for the ADC input.

TYPICAL CIRCUIT CONNECTION

Figure 33 illustrates typical circuit connection.



Note: C1, C2: 0.1-μF ceramic capacitor and 10-μF electrolytic capacitor, depend on power supply.

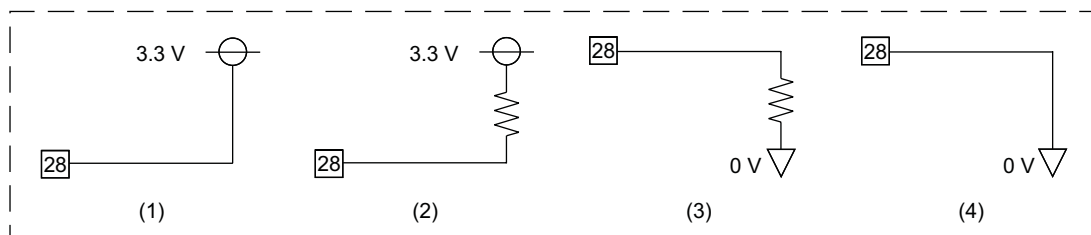
C3: 0.1-μF ceramic capacitor and 10-μF electrolytic capacitor is recommended.

C4, C5: 4.7-μF electrolytic capacitor is recommended for 3-Hz cutoff frequency.

The termination for mode/configuration control.

Either one of following circuits has to be applied according to necessary mode/configuration.

Resistor value must be 220 kΩ, ±5 % tolerance.

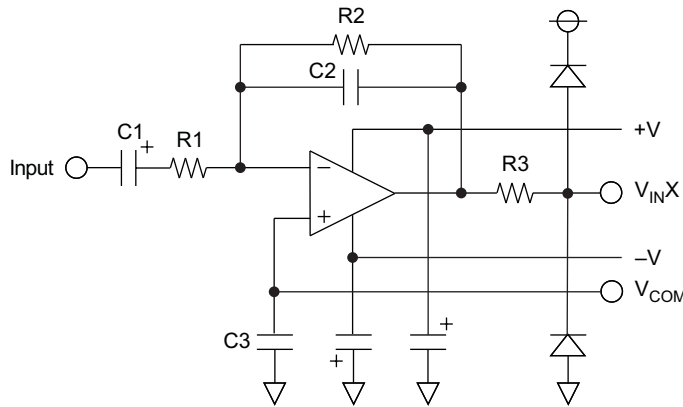


S0257-01

Figure 33. Typical Application Diagram

Application Examples for Analog Input and Output

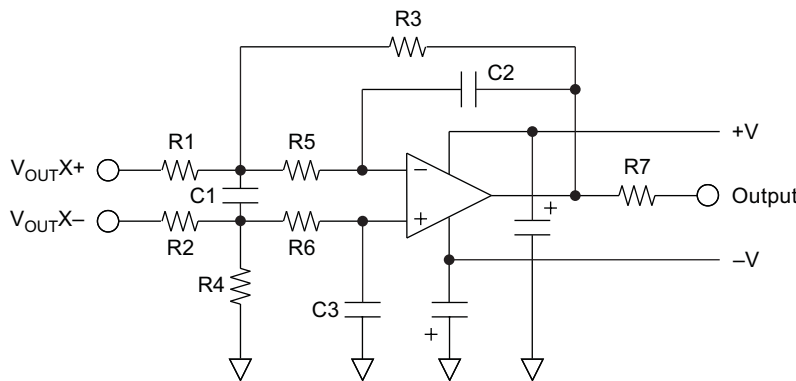
a) Example of V_{COM} -biased buffering for 2-Vrms input with overvoltage protection.



Example of C, R values with gain (G) and corner frequency (f_C)

- R1: 20 k Ω
- R2: 10 k Ω
- R3: 1 k Ω
- C1: 10 μ F
- C2: 330 pF
- C3: 0.1 μ F
- G: 0.5
- f_C : 48 kHz

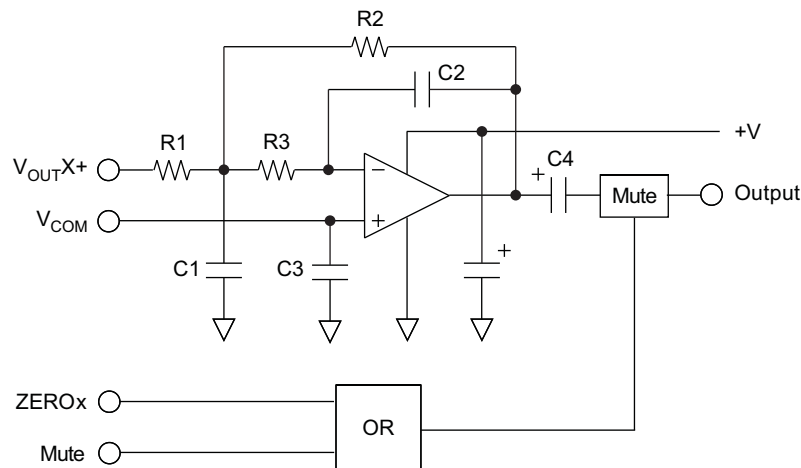
b) Example of capless differential to single-ended converter with LPF and gain for 2-Vrms standard output.



Example of C, R values with gain (G) and corner frequency (f_C)

- R1, R2: 10 k Ω
- R3, R4: 7.5 k Ω
- R5, R6: 820 Ω
- R7: 100 Ω
- C1: 1500 pF
- C2, C3: 470 pF
- G: 0.75 (Differential to S/E)
- f_C : 54 kHz

c) Example of V_{COM} -biased single-supply single-ended application with LPF and MUTE control for 1-Vrms output.



Example of C, R values with gain (G) and corner frequency (f_C)

- R1: 10 k Ω
- R2: 7.5 k Ω
- R3: 750 Ω
- C1: 3300 pF
- C2: 470 pF
- C3: 0.1 μ F
- C4: 10 μ F
- G: 0.75
- f_C : 54 kHz

Figure 34. Application Examples for Analog Input and Output

S0258-01

DESIGN AND LAYOUT CONSIDERATIONS IN APPLICATION

Power Supply Pins (V_{CC} , V_{DD})

The digital and analog power supply lines to the PCM3060 should be bypassed to the corresponding ground pins with 0.1- μ F ceramic and 10- μ F electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC and DAC.

Although the PCM3060 has two power lines to maximize the potential of dynamic performance, using one common source, 5-V power supply for V_{CC} and a 3.3-V power supply for V_{DD} which is generated from the 5-V power supply for V_{CC} , is recommended to avoid unexpected problems, such as latch-up, from incorrect power supply sequencing.

Grounding (AGND1, AGND2, SGND, DGND)

To maximize the dynamic performance of the PCM3060, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise and signal components feeding back into the analog ground. So, they should be connected directly to each other under the parts to reduce the potential of noise problems.

V_{INL} , V_{INR} Pins

A 4.7- μ F electrolytic capacitor is recommended as the ac coupling capacitor, which gives a 3-Hz cutoff frequency. If higher full-scale input voltage is required, it can be adjusted by adding only one series resistor to the V_{INX} pins, although a small gain error is added due to variations of absolute input resistance of the PCM3060. For example, adding 9.1 k Ω gives 2 V_{rms} full-scale with about 10% gain error.

V_{COM} Pin

Ceramic 0.1- μ F and electrolytic 10- μ F capacitors are recommended between V_{COM} and AGND to ensure low source impedance of the ADC and DAC references. These capacitors should be located as close as possible to the V_{COM} pins to reduce dynamic errors on ADC and DAC references.

V_{OUTL+} , V_{OUTL-} , V_{OUTR+} , V_{OUTR-} Pins

The differential to single-ended buffer with post LPF can be directly (without capacitor) connected to these output pins, thereby minimizing the use of coupling capacitors for the 2-V_{rms} outputs. The output pins in single-ended mode are assigned to V_{OUTL+} and V_{OUTR+} ; in single-ended mode, the V_{OUTL-} and V_{OUTR-} pins must be open.

MODE Pin

This pin is a logic input with quad-state input capability.

The pin is connected to V_{DD} for High, to DGND for Low, and pulled up or pulled down through an external resistor and for the two mid-states in order to distinguish the four input states. The pullup or pulldown resistor must be 220 k Ω , \pm 5% tolerance.

System Clocks

The quality of SCK11/2 may influence dynamic performance, as the PCM3060 (both ADC and DAC) operates based on SCK11/2. Therefore, it may be required to consider the jitter, duty, rise and fall time, etc. of the system clocks.

The PCM3060 supports asynchronous operation between the ADC and DAC. Therefore, there is no restriction on the relationship between SCK11 and SCK12 for digital operation, but it is strongly recommended to use a common clock if the application does not require different base clock frequencies, like 44.1 kHz and 48 kHz.

Audio Interface Clocks

In slave mode, PCM3060 does not require specific timing relationship between BCK1/LRCK1 and SCK11, BCK2/LRCK2 and SCK12, but there is a possibility of performance degradation with a certain timing relationship between them. In that case, specific timing-relationship control might solve this performance degradation.

In master mode, there is a possibility of performance degradation due to heavy loads on BCK1/LRCK1, BCK2/LRCK2 and DOUT. It is recommended to load these pins as lightly as possible.

External Mute Control

For power-down ON/OFF control without the pop noise which is generated by a dc level change on the DAC output, the external mute control is generally required. Use of the following control sequence is recommended: external mute ON, codec power down ON, SCK11/SCK12 stop and resume if necessary, codec power down OFF, and external mute OFF.

REVISION HISTORY

| Changes from Original (March 2007) to Revision A | Page |
|---|------|
| <ul style="list-style-type: none"> Changed Figure 34(a), (b), and (c). Updated the Example of C, R values. | 40 |
| Changes from Revision A (February 2008) to Revision B | Page |
| <ul style="list-style-type: none"> Changed Supply Current - $f_s = 48$ kHz/ADC, $f_s = 48$ kHz/DAC max value From: 30 mA To: 36 mA Changed Power dissipation - $f_s = 48$ kHz/ADC, $f_s = 48$ kHz/DAC max value From: 190 mW To: 220 mW | 6 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| PCM3060PW | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | PCM3060 | Samples |
| PCM3060PWG4 | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | PCM3060 | Samples |
| PCM3060PWR | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | PCM3060 | Samples |
| PCM3060PWRG4 | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -25 to 85 | PCM3060 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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MECHANICAL DATA

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

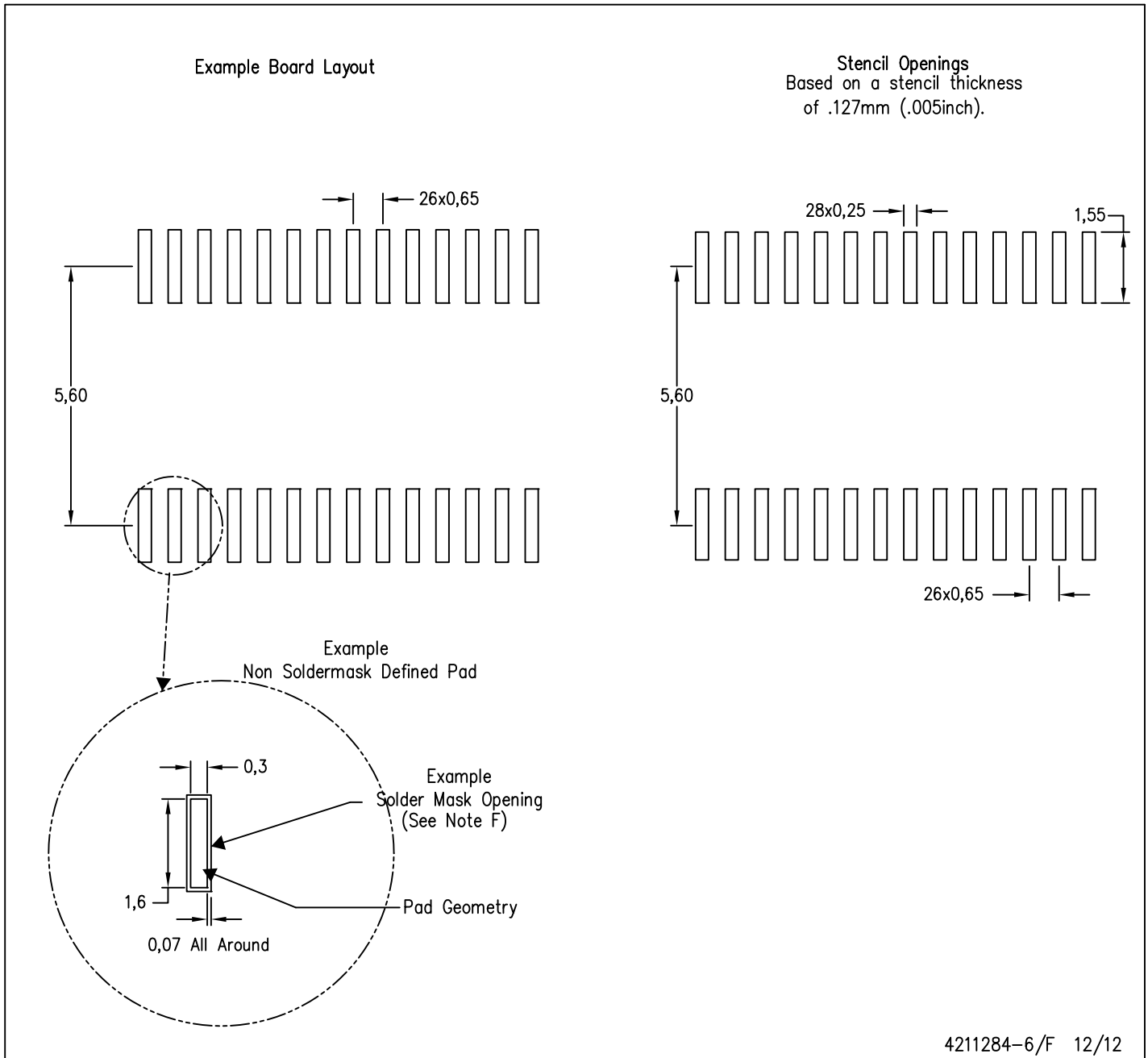


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

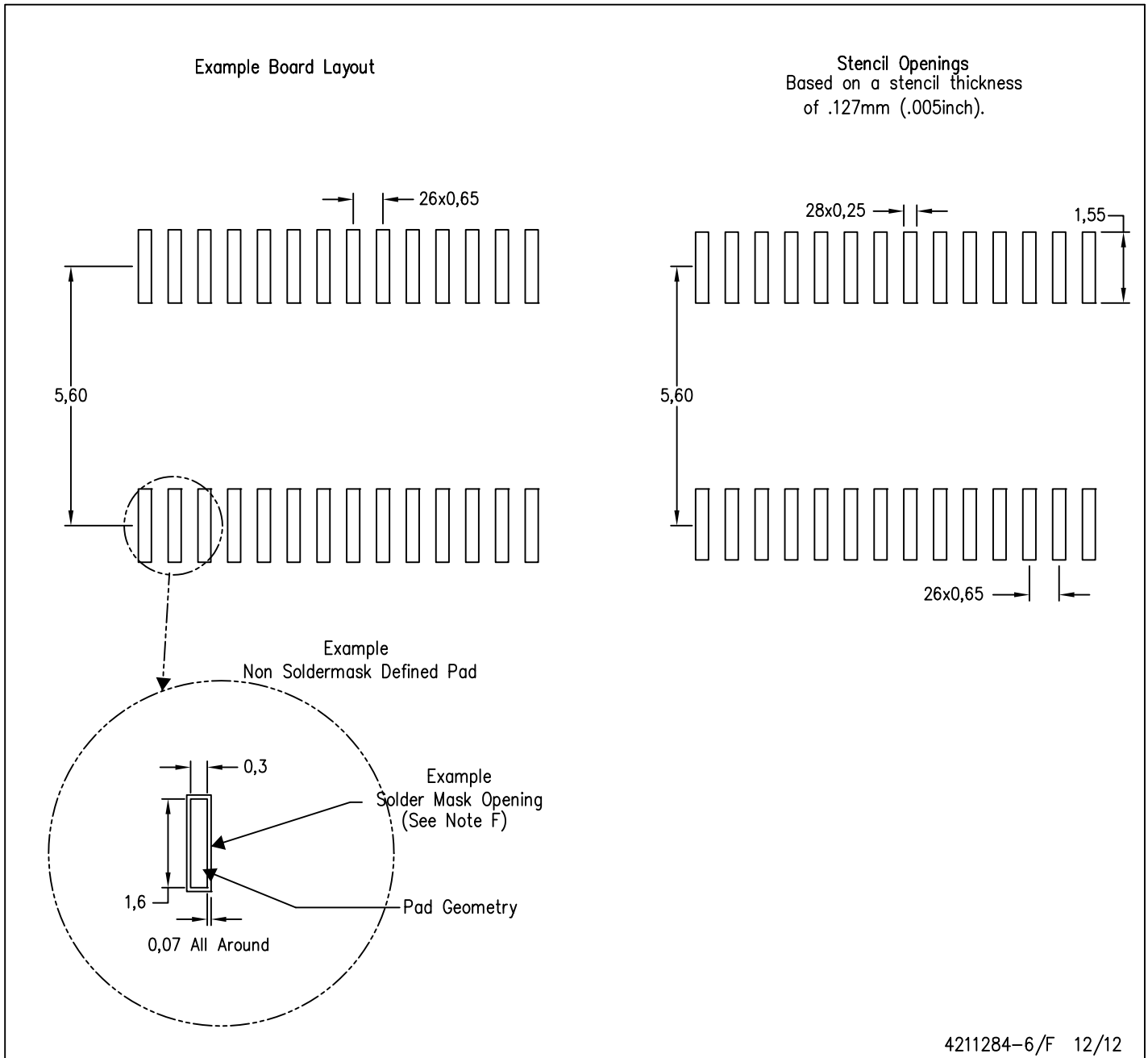


4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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