深圳市拓普微科技开发有限公司
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LMT035KDH03

LCD Module User Manual

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K.C.		
Date: 2012-04-17	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary	2009-09-27
0.2	Typing Correction on Terminals Table	2010-04-03
0.3	Update Parameters	2012-01-31
0.4	Add T_{VS} timing details and typical input data timing diagram in 5.3.1	2012-04-17

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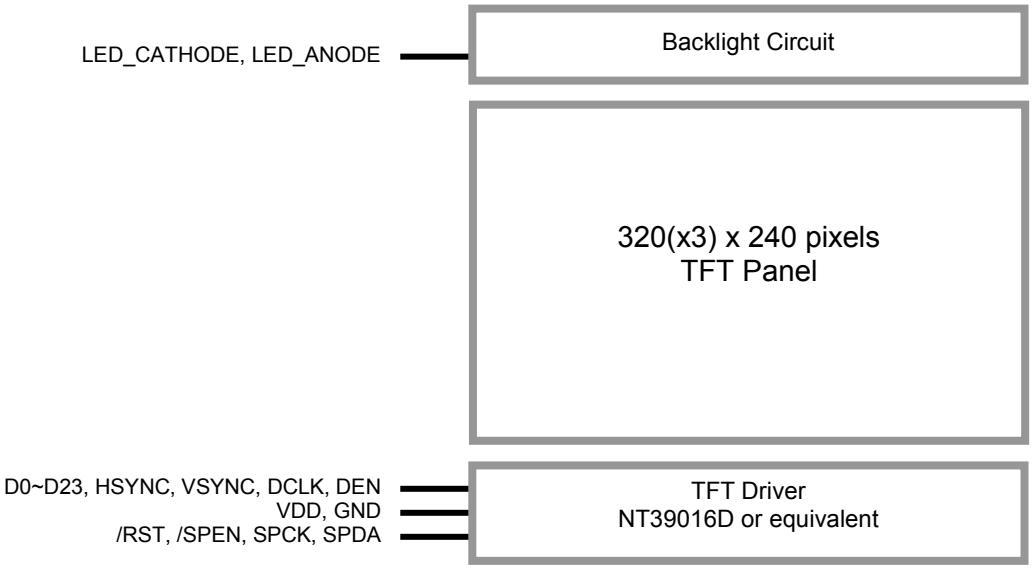
1. General Specification

Screen Size(Diagonal) :	3.5 inch
Resolution :	320(RGB) x 240
Signal Interface :	24bit parallel bus / CCIR656 / 601
Color Depth :	16.7M color (24bit) *1
Dot Pitch :	0.219 x 0.219 (mm)
Pixel Configuration :	RGB Stripe
Display Mode :	Transmissive / Positive
Surface Treatment :	Anti-Glare Treatment
Viewing Direction :	12 o'clock
Outline Dimension :	76.9 x 63.9 x 3.15 (mm) (exclude FPC, see attached drawing for details)
Active Area :	70.08 x 52.56 (mm)
Weight :	(29.3g)
Backlight :	6 LEDs (in series)
Driver IC	NT39016D
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:
*1 Color tune may slightly changed by temperature and driving voltage.

2. Block Diagram



3. Terminal Functions

3.1 Interface

Pin No.	Pin Name	I/O	Descriptions
1	LED_CATHODE	P	Backlight LED Cathode supply
2			
3	LED_ANODE	P	Backlight LED Anode supply
4			
5	NC	-	No Connection
6	NC	-	
7	NC	-	
8	/RST	I	Reset signal active LOW
9	/SPEN	I	SPI enable signal, active LOW, normal HI (*1)
10	SPCK	I	SPI clock signal, rising edge trigger(*1)
11	SPDA	I/O	SPI data signal (*1)
12	D0	I	B0~B7, Blue data input(*2)
:	:		
19	D7		
20	D8	I	G0~G7 Green data input (*2)
:	:		
27	D15		
28	D16	I	R0~R7(*2) Read data input (*2)
:	:		
35	D23		
36	HSYNC	I	Horizontal Sync Signal
37	VSYNC	I	Vertical Sync Signal
38	DCLK	I	Data Clock Input
39	NC	--	No Connection
40	NC	--	
41	VDD	P	Positive Power Supply
42	VDD		
43	NC	--	No Connection
:	:		
51	NC		
52	DEN	I	Data Enable Input (*3)
53	GND	P	Power Ground Supply
54	GND		

Note:

*1. /SPEN, SPCK, SPDA must be connected to referenced control pins to enable the SPI initialization
It may necessary to config the TFT Driver through SPI interface to provide best display result.

*2. For CCIR601/CCIR656 Interface, only R0-R7 is used. For unused pins (B0-B7,G0-G7), please connect to GND or floating. The interface is selected by the SPI initial code.
Default setting is parallel 24-bit RGB interface.

Mode	D(23:16)	D(15:08)	D(07:00)	HSYNC	VSYNC	DEN
ITU-R BT 656	D(23:16)	GND	GND	NC	NC	NC
ITU-R BT 601	D(23:16)	GND	GND	HSYNC	VSYNC	NC
8 Bit RGB	D(23:16)	GND	GND	HSYNC	VSYNC	NC for HV Mode
						DEN for Den Mode
24 Bit RGB	R(7:0)	G(7:0)	B(7:0)	HSYNC	VSYNC	NC for HV Mode
						DEN for Den Mode

*3: For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported.
If DEN signal is fixed low. SYNC mode is used. Otherwise, DE+SYNC is used

4. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+4.0	V	GND = 0V
Input Voltage	V_{IN}	-0.3	+4.0	V	GND = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

5. Electrical Characteristics

5.1 DC Characteristics (MCU terminal)

GND=0V, V_{DD} =3.3V, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	V_{DD}	3.0	3.3	3.6	V	VDD
Input High Voltage	V_{IH}	0.8VDD	-	VDD	V	Input pins
Input Low Voltage	V_{IL}	GND	-	0.2VDD	V	Input pins
Frame Freq	F_{FRAME}	-	60	-	Hz	
Dot Data Clock(*1)	f_{DOTCLK}	-	6.5	-	MHz	
Operating Current(*2)	I_{DD}	6.5	7.4	9.4	mA	VDD

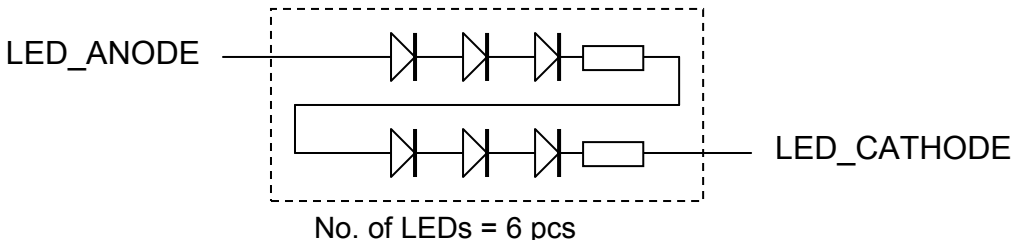
Note.
*1. DOTCLK must be adapted to 19.5MHz in 8-bit mode
*2. test image is 16-grayscaly graphic

5.2 LED Backlight Circuit Characteristics

$If_{LED\ ANODE}$=20mA, T_{OP}=25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Note
Forward Voltage	$Vf_{LED\ ANODE}$	-	19.2	-	V	
Forward Current	$If_{LED\ ANODE}$	-	20	25	mA	
Life Time	-	-	(50000)	-	hr	

Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



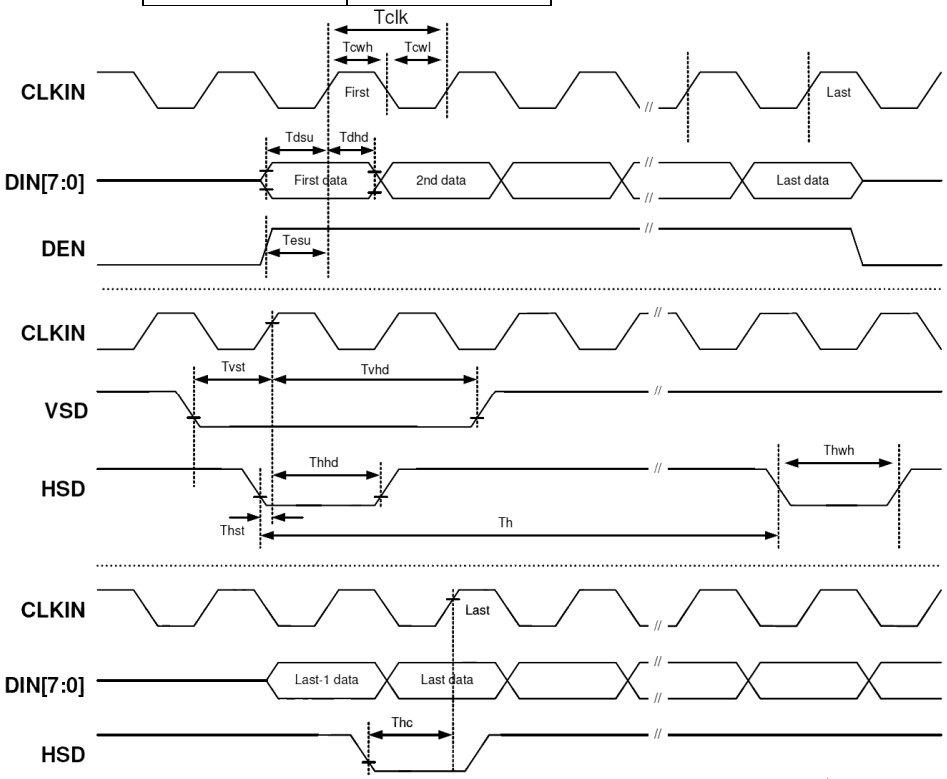
5.3 AC Characteristics

5.3.1 Display Data Input Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD power source slew time	T_{POR}			1000	us	From 0V to 90% VDD
RSTB active pulse width	T_{RSTB}	40			us	VDD = 3.3V
CLKIN clock time	Tclk	33.3/125	-	-	ns	Please refer to timing table(p.32)
HSD to CLKIN	Thc	-	-	1	CLKIN	
HSD width	Thwh	1	-	-	CLKIN	
VSD width	Tvwh	1	-	-	Th	
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	8	-	-	ns	
VSD hold time	Tvhd	10	-	-	ns	
HSD setup time	Thst	8	-	-	ns	
HSD hold time	Thhd	10	-	-	ns	
Data set-up time	Tdsu	8	-	-	ns	DIN[23:0] to CLKIN
Data hold time	Tdhd	10	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	Tesd	12	-		ns	DEN to CLKIN
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@CCIR601 / 8bit RGB HV mode Control by HDLY[6:0] setting Tvs = HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting Tvs = HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	17	25	33	Th	@CCIR656 PAL mode Control by HDLY[6:0] setting Tvs = HDLY[6:0]
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting Tvs = HDLY[6:0]

Signal naming references:

Terminal Name	Signal Name
D23~D0	DIN[23:0]
DCLK	CLKIN
HSYNC	HSD
VSYNC	VSD
DEN	DEN



Timing Diagram

CCIR601 mode A/B

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	24.54 /27	30	MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	-	40/37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time from HSD to 1'st data input (PAL)	Ths	128	264	-	CLKIN	DDLY = 136, Offset = 128 (fixed)
Time from HSD to 1'st data input (NTSC)	Ths	128	244	-	CLKIN	DDLY = 116, Offset = 128 (fixed)

CCIR656 mode A/B

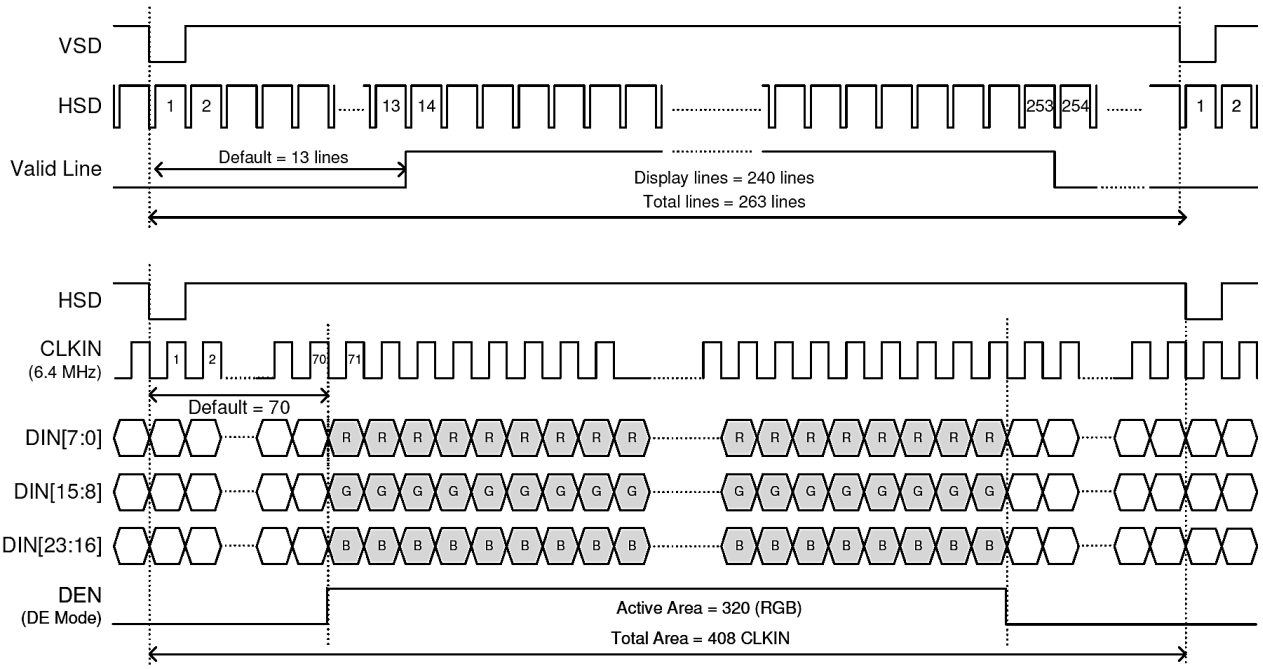
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27	30	MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	-	37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time from EAV to 1'st data input (PAL)	Ths	128	288		CLKIN	DDLY = 152, Offset = 128 (fixed)
Time from EAV to 1'st data input (NTSC)	Ths	128	276		CLKIN	DDLY = 140, Offset = 128 (fixed)

8bit RGB 960 CH Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27	30	MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	-	37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1'st data input(NTSC)	Ths	35	70	255	CLKIN	DDLY = 70, Offset = 0 (fixed)

24bit RGB mode (SEL[3:0]=1100 or 1101)

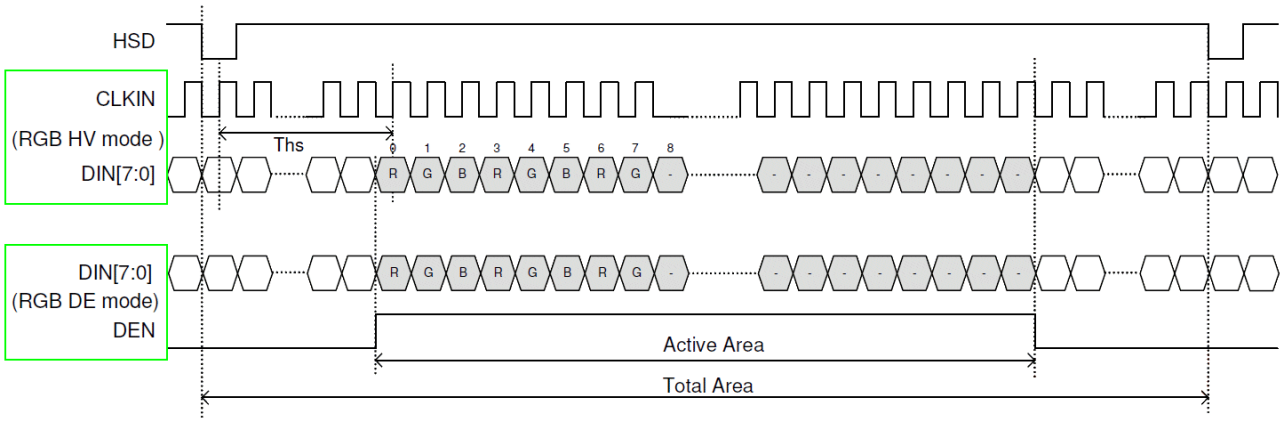
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	6.1	6.4	8.0	MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	125	156	164	ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1'st data input(NTSC)	Ths	40	70	255	CLKIN	DDLY =70, Offset = 0 (fixed)



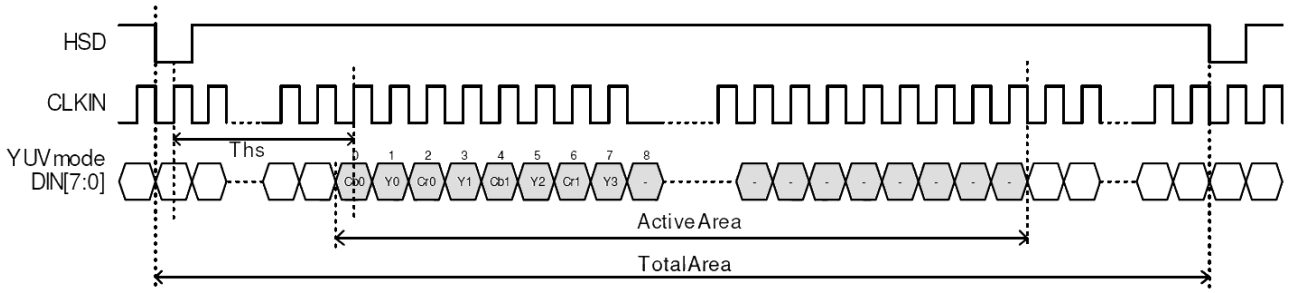
Typical Input Data Timing Diagram (24bit RGB mode SEL[3:0]=1100)

5.3.2 Active Display Timing

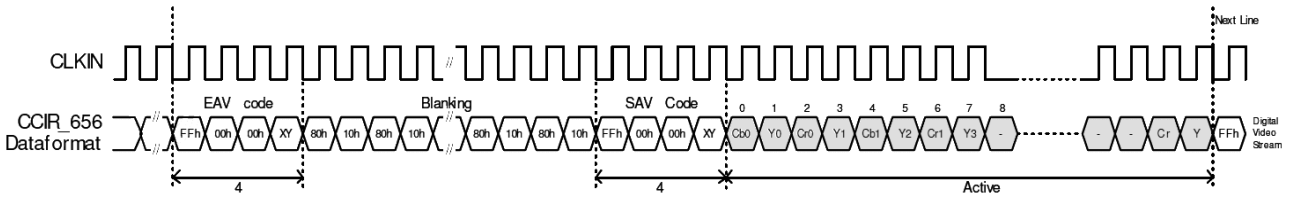
Input Format	Format Standard	CLKIN (MHz)	HSD (CLKIN)	Total Area (CLKIN)	Active Area (CLKIN)	Note
YUV	CCIR_601	27	1	1716	1440	
	CCIR_656			1728		
	CCIR_601	24.54	1	1560	1280	
8bit RGB	8 bit RGB	27	1	1716	960	960x240
24bit RGB	24 bit RGB	6.4	1	408	320	



RGB input Data Format



YUV input Data Format



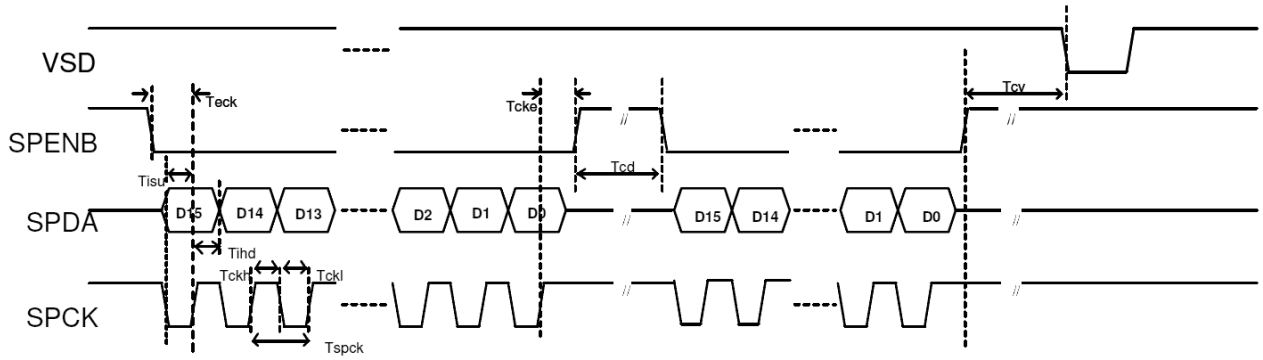
CCIR_656 input Data Format

5.3.3 SPI Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Serial clock	Tspck	320	-	-	ns	
SPCK pulse duty		40	50	60	%	Tckh / Tspck
Serial data setup time	Tisu	120	-	-	ns	
Serial data hold time	Tihd	120	-	-	ns	
Serial clock high/low	Tckh/l	120	-	-	ns	
Chip select distinguish	Tcd	1	-	-	us	
SPENB to VSD	Tcv	1	-	-	us	
SPENB input setup time	Teck	150	-	-	ns	
SPENB input hold time	Tcke	150	-	-	ns	

Signal naming references:

Terminal Name	Signal Name
SPDA	SPDA
SPCK	SPCK
VSYNC	VSD
/PSEN	PSENB
/RST	RSTB



Timing Diagram

6. Optical Characteristics

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		θ=0° Φ=0°	-	250	-	Cd/m^2	1
Uniformity	△Bp			80%	-	-		1,2
Viewing Angle	θ1 (Φ=90° or270°)		Cr≥10	-25～+60			Deg	3
	θ2 (Φ=0° or 180°)			-45～+45				
Contrast Ratio	Cr		θ=0° Φ=0°	-	300	-	-	4
Response Time	T_r			-	25	40	ms	5
	T_f			-	25	40	ms	
Color of CIE Coordinate	W	x	θ=0° Φ=0°	-	0.29	-	-	1,6
		y		-	0.31	-	-	
	R	x		-	0.60	-	-	
		y		-	0.37	-	-	
	G	x		-	0.34	-	-	
		y		-	0.57	-	-	
	B	x		-	0.15	-	-	
		y		-	0.09	-	-	
NTSC Ratio	S			50	-		%	

Note：The parameter is slightly changed by temperature, driving voltage and materiel.

Note 1:
The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)
Measuring condition:
- Measuring surroundings: Dark room
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

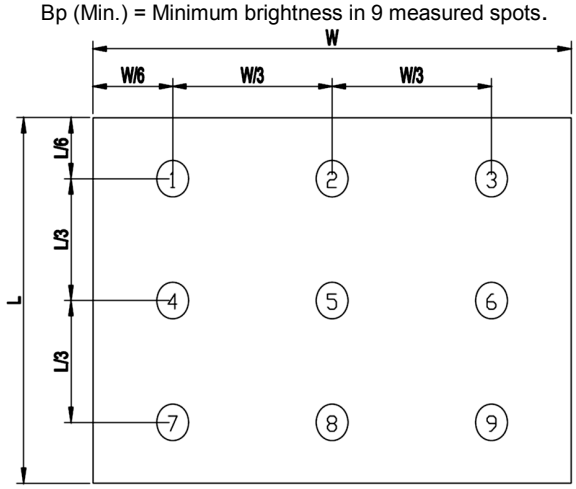
Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

Note 2:
The luminance uniformity is calculated by using following formula.

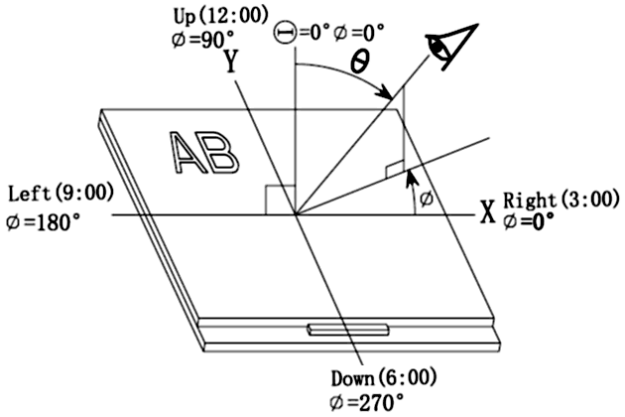
△Bp = Bp (Min.) / Bp (Max.)×100 (%)

Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.



Note 3:
The definition of viewing angle:
Refer to the graph below marked by θ and Φ

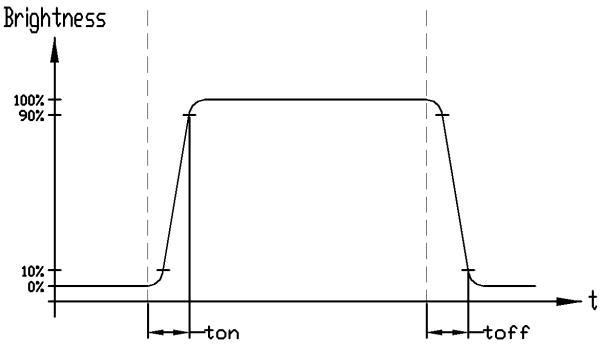


Note 4:
The definition of contrast ratio (Test LCM using PR-705):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

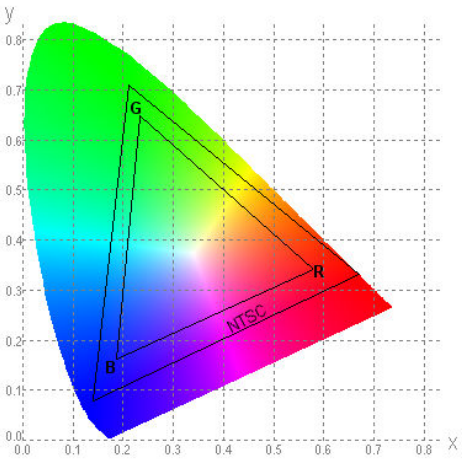
Note 5:
Definition of Response time. (Test LCD using DMS501):
The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



Note 6:
Definition of Color of CIE Coordinate and NTSC Ratio.

Color gamut:

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

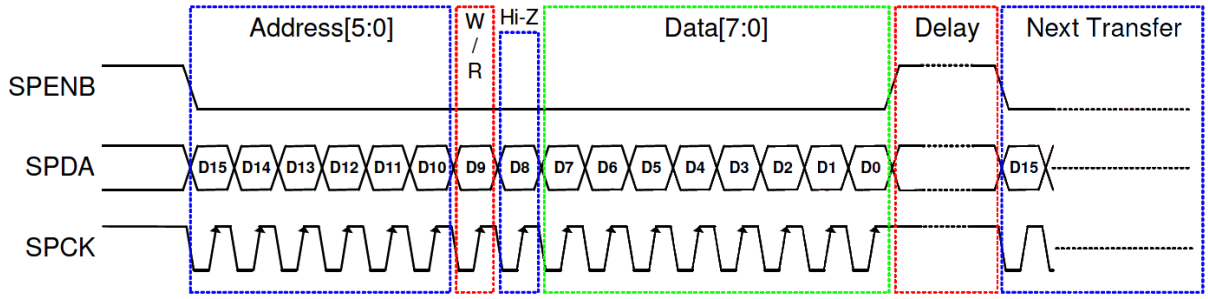


7. Function Specifications

7.1 SPI Interface Command Packet

The LMT035KDH03 terminal equipped with a SPI interface, which is for receiving command to adjust the TFT display to the best display result.

Command packet is in 16bit format, which include Register Address and Register Data.
/SPEN works as a chip enable pin and also for init the communication.
PSDA is the serial data line
SPCK is the serial clock, data bit latches into the TFT driver at rising edge



3-Wire Command Format:

Bit	Description
D15-D10	Register Address [5:0].
D9	W/R control bit. “1” for Write; “0” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	X	DATA (Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	Hi-Z	DATA (Issue by NT39016)							

7.2 SPI Interface Commands Summary

3-Wire Registers		Register Description		
D[15:10]	Name	Init.	R/W	Function Description
000000b	R00	07h	R/W	System control register
000001b	R01	00h	R/W	Timing Controller function register
000010b	R02	03h	R/W	Operation control register
000011b	R03	CCh	R/W	Input data Format control register
000100b	R04	46h	R/W	Source Timing delay control register
000101b	R05	0Dh	R/W	Gate Timing delay control register
000110b	R06	00h	R/W	Reserved
000111b	R07	00h	R/W	Internal function control register
001000b	R08	08h	R/W	RGB Contrast control register
001001b	R09	40h	R/W	RGB Brightness control register
001010b	R0A	88h	R/W	Hue / Saturation control register
001011b	R0B	88h	R/W	R / B Sub-Contrast control register
001100b	R0C	20h	R/W	R Sub-Brightness control register
001101b	R0D	20h	R/W	B Sub-Brightness control register
001110b	R0E	10h	R/W	VCOMDC Level Control Register
001111b	R0F	A4h	R/W	VCOMAC Level Control Register
010000b	R10	04h	R/W	VGAM2 level control register
010001b	R11	24h	R/W	VGAM3/4 level control register
010010b	R12	24h	R/W	VGAM5/6 level control register
100000b	R20	00h	R/W	Wide and narrow display mode control register

7.3 SPI Interface Commands Details

R00: System Control Register

Bit	Name	Initial	R/W	Description
Bit [7:4]	PAT[3:0]	0000b	R/W	Internal Test Pattern Selection PAT[3:0] : Select chip embedded test pattern.
Bit [3]	PWMPDB	0b	(R) R/W	Internal PWM controller Power Down bit PWMPDB = “0”, internal PWM controller will be shut down PWMPDB = “1”, internal PWM controller normal operating
Bit [2]	-	-	-	Reserve
Bit [1]	STBYB	1b	(R) R/W	Standby Mode function control. STBYB = “0”, TCON, Source output will turn off and outputs are High-Z. STBYB = “1”, Normal operation
Bit [0]	RESETB	1b	R/W	Global Reset Register. Write “0” to reset whole chip. This bit will set to “1” automatically after chip was reset.

PAT[3:0] : Embedded Auto Test Pattern Selection Register

PAT[3:0]	Test Pattern	Note
00H	Disable Internal Test Pattern Function	Default
01H	White	
02H	Black	
03H	Red	
04H	Green	
05H	Blue	
06H	Yellow	
07H	Cyan	
08H	Magenta	
09H	Gray Level 8	
0AH	Gray Level 16	
0BH	Color Bar	
0CH	Checker Board	
0DH	Cross Talk Pattern	
0EH	Horizontal Flick Pattern	
0FH	Test Pattern Auto Run Mode	

Note: WNSEL[1:0] will be disabled under Internal Test Pattern mode.

R01: Timing Controller Function Register

Bit	Name	Initial	R/W	Description
Bit [4:2]	SWD[2:0]	000b	R/W	Control and switch the relationship between the R,G,B and outputs. This register is used to match different types of color filters on LCD panel
Bit [1]	DITHB	0b	R/W	Dithering enable. Active low DITHB = "0", Dithering on, (Pseudo 8-bits resolution). (Default mode) DITHB = "1", Dithering off, (6-bits resolution, truncation last 2-bits of the input data) Note 1: Recommend user to enable this function under all modes except for 18 bit RGB input application.
Bit [0]	CFTYP	0b	R/W	Color Filter Type Select. Select Delta or Stripe mode for data arrangement. CFTYP = "0", Stripe mode, Data arrangement keep in the "odd line" state of SWD[2:0] selection. CFTYP = "1", Delta mode, Data arrangement controlled by SWD[2:0] setting.

SWD[2:0] function control:

SWD2	SWD1	SWD0	Output (n=0 to 319)				Condition
			3n+1	3n+2	3n+3		
0	0	0	R	G	B	Odd Line	SHLR="1" UPDN="1"
			G	B	R	Even Line	
0	0	1	G	B	R	Odd Line	
			B	R	G	Even Line	
0	1	X	B	R	G	Odd Line	
			R	G	B	Even Line	
1	0	0	G	B	R	Odd Line	
			R	G	B	Even Line	
1	0	1	B	R	G	Odd Line	
			G	B	R	Even Line	
1	1	X	R	G	B	Odd Line	
			B	R	G	Even Line	

Note 1: X = Don't care
Note 2: Data arrangement will keep in the "odd line" state when CFTYP = 0 for stripe mode.

R02: Operation Control Register

Bit	Name	Initial	R/W	Description
Bit [7]	SKIPMOD	0b	(R) R/W	Horizontal data processing algorithms select register. SKIPMOD = "0": Horizontal data weighting skip mode. (Default mode) SKIPMOD = "1": Horizontal data direct skip mode.
Bit [6:5]	HDNC[1:0]	00b	(R) R/W	Horizontal Data scaling mode select register. This function is active under CCIR601 and CCIR656 mode only.
Bit [4]	-	-	-	Reserve
Bit [3]	FPOL	0b	R/W	VCOMOUT polarity inverse control. FPOL = "0": VCOMOUT normal polarity (Default mode). FPOL = "1": VCOMOUT inverse polarity.
Bit [2]	VSET	0b	R/W	Gamma correction source select. VSET = "0", used internal Gamma Reference voltage (VDDA). (Default mode) VSET = "1", used external Gamma Reference Input (V1~V7).
Bit [1]	UPDN	1b	(R) R/W	Gate Driver Up/down scan control of gate driver. UPDN = "0", Shift from down to up, First line=L240->L239->,,->L2->L1= Last line UPDN = "1", Shift from up to down, First line=L1->L2->,,->239->240= Last line (Default mode)
Bit [0]	SHLR	1b	(R) R/W	Right/Left sequence control of source driver. SHLR = "0", shift left: Last data = S1< S2< S3.....< S960 =First data. SHLR = "1", shift right: First data = S1 >S >S3..... >S960 = Last data.

HDNC[1:0] function setting for different horizontal data skip mode

HDNC1	HDNC0	Source Data	Data Skip Mode
0	0	1440 / 1280 clock	1440 clock -> 720 RGB -> (scale down) 320 RGB 1280 clock -> 640 RGB -> (scale down) 320 RGB
0	1	1440 clock	1440 clock -> 720 RGB -> (Skip Right/Left 10 RGB) 700 RGB -> (scale down) 320 RGB
1	0	1440 clock	1440 clock -> 720 RGB -> (Skip Right/Left 20 RGB) 680 RGB -> (scale down) 320 RGB
1	1	1440 clock	1440 clock -> 720 RGB -> (Skip Right/Left 40 RGB) 640 RGB -> (scale down) 320 RGB

Note: HDNC function is active under CCIR601/656 mode only

R03: Input Data Format Control Register

Bit	Name	Initial	R/W	Description
Bit [7]	DENPOL	1b	R/W	DEN input pin polarity control. DENPOL = "0", DEN negative polarity. DENPOL = "1", DEN positive polarity. (Default mode)
Bit [6]	CLKPOL	1b	R/W	CLKIN pin polarity control. CLKPOL = "0", CLKIN negative edge latch data. CLKPOL = "1", CLKIN positive edge latch data. (Default mode)
Bit [5]	HSDPOL	0b	R/W	HSD pin polarity control. HSDPOL = "0", HSD negative polarity. (Default mode) HSDPOL = "1", HSD positive polarity.
Bit [4]	VSDPOL	0b	R/W	VSD pin polarity control. VSDPOL = "0", VSD negative polarity. (Default mode) VSDPOL = "1", VSD positive polarity
Bit [3:0]	SEL[3:0]	1100b	(R) R/W	Input data format selection. Note: Different SEL [3:0] setting resolute in different AC timing.

SEL[3:0]: Data input mode

SEL3	SEL2	SEL1	SEL0	Data input format	Operating frequency
0	0	0	0	CCIR601 YUV 1280 input format (YUV mode A)	24.54 MHz
0	0	0	1	CCIR601 YUV 1280 input format (YUV mode B)	24.54 MHz
0	0	1	0	CCIR601 YUV 1440 input format (YUV mode A)	27 MHz
0	0	1	1	CCIR601 YUV 1440 input format (YUV mode B)	27 MHz
0	1	0	0	CCIR656 YCbCr input format (YcbCr mode A)	27 MHz
0	1	0	1	CCIR656 YCbCr input format (YcbCr mode B)	27 MHz
0	1	1	0	-	-
0	1	1	1	-	-
1	0	0	0	8-bit digital RGB input format HV Mode (NTSC only)	27 MHz
1	0	0	1	8-bit digital RGB input format DE Mode (NTSC only)	27 MHz
1	0	1	0	8-bit digital RGB through mode input format HV Mode (NTSC only)	27 MHz
1	0	1	1	8-bit digital RGB through mode input format DE Mode (NTSC only)	27 MHz
1	1	0	0	24-bit digital RGB input format HV Mode (NTSC only)	6.4 MHz
1	1	0	1	24-bit digital RGB input format DE Mode (NTSC only)	6.4 MHz
1	1	1	0	-	-
1	1	1	1	-	-

Note：Hsync and Vsync will be floated in CCIR656 and DE mode
Remark:
YUV mode A: Data sequence are "Cb_Y_Cr_Y…".
YUV mode B: Data sequence are "Cr_Y_Cb_Y…".
RGB through mode will bypass 3-wire SWD[2:0] function;TCON will not arrange data color mapping.

R04: Source Timing Delay Control Register

Bit	Name	Initial	R/W	Description
Bit [7:0]	DDLY[7:0]	46h	R/W	Select the HSD signal to 1'st input data delay timing Under CCIR601 mode, Ths = DDLY[7:0] + 128, (Unit = CLKIN) Under CCIR656 mode, Ths = DDLY[7:0] + 136, (Unit = CLKIN) Under RGB 8/24 bit mode, Ths = DDLY[7:0] , (Unit = CLKIN) The register value will be update to the different default value each time when SEL[3:0] changed. Read the section of "Timing Table" for the detail, please.

Note: DDLY function will be disabled under 8/24bit DE mode and PINCTLB = 0 condition. The default value list in the timing table will be used when PINCTLB = 0.

R05: Gate Timing Delay Control Register

Bit	Name	Initial	R/W	Description
Bit [7]	-	-	-	Reserve
Bit [6:0]	HDLY[6:0]	0Dh	R/W	Select the Gate start pulse output delay timing Tvs = HDLY[6:0], (Unit = HSD) The register value will be update to the different default value each time when SEL[3:0] changed. Read the section of "Timing Table" for the detail, please.

Note: HDLY function will be disabled under 8/24bit DE mode and PINCTLB = 0 condition. The default value list in the timing table will be used when PINCTLB = 0.

R06: Reserved

Bit	Name	Initial	R/W	Description
Bit [7:0]	-	-	-	Reserve

R07: Internal Function Control Register

Bit	Name	Initial	R/W	Description
Bit [7:6]	FRAD[1:0]	00b	R/W	Odd frame or Even frame advance control
Bit [5:4]	INVSL[1:0]	00b	R/W	Source Driving Mode Selection Register
Bit [3]	PAL	0b	(R) R/W	NTSC or PAL mode selection. Only for 601 and 656 mode. PAL = "0", Select NTSC interface mode. (Default mode) PAL = "1", Select PAL interface mode.
Bit [2]	PALM	0b	(R) R/W	PAL mode input data format selection PALM = "0", Select PAL 280 line mode. (Default mode) PALM = "1", Select PAL 288 line mode
Bit [1]	-	-	-	Reserve
Bit [0]	AVGY	0b	R/W	Average YUV interface Luminance Y. AVGY = "0"; Only used odd Y sample for YUV conversion, AVGY = "1"; Used odd and even Y sample for YUV conversion. This function active under YUV mode only!

INVSL[1:0]

INVSL1	INVSL0	Driving Mode	Notes
0	0	1 - Line Inversion	Default
0	1	2 - Line Inversion	
1	0	Frame Inversion	
1	1	Reserved	

FRAD[1:0]

FRAD1	FRAD0	Advance Frame	Notes	
0	0	Default	Odd/Even frame Tstv are the same	Unit: H
0	1	Odd frame	Even frame Tstv = HDLY setting +1	
1	0	Even frame	ODD frame Tstv = HDLY setting +1	
1	1	Reserve	Reserve	

Note: Remark: This function is available under CCIR601 and CCIR656 mode only.

R08: Contrast Control Register

Bit	Name	Initial	R/W	Description
Bit [7:5]	-	-	-	Reserve
Bit [4:0]	CON[4:0]	08h	R/W	Display Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0) to 0x1F(level = 3.875) Default value 08h(level = 1.0)

R09: Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit [7]	-	-	-	Reserve
Bit [6:0]	BRI[6:0]	40h	R/W	Display Brightness level adjustment register. (2/Step) Adjust range from 0x00(level = -128) to 0x7F(level = +126) Default value 0x40(level = +0)

R0A: Hue and Saturation Control Register

Bit	Name	Initial	R/W	Description
Bit [7:4]	HUE[3:0]	08h	R/W	YUV Hue level adjustment register. (5 Deg/Step) Adjust range from 0x00(level = -40 Deg) to 0x0F(level = +35 Deg) Default value 0x08(level = 0 Deg) Cb' = Cb * cos θ + Cr * sin θ Cr' = Cr * cos θ + Cb * sin θ
Bit [3:0]	SAT[3:0]	08h	R/W	YUV saturation level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0) to 0x0F(level = 1.875) Default value 0x08(level = 1.00)

Note: Hue and Saturation function was available under YUV input mode only.

R0B: R / B Sub-Contrast Control Register

Bit	Name	Initial	R/W	Description
Bit [7:6]	SCONB[1:0]	02h	R/W	B Data Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0.75) to 0x0F(level = 1.125) Default value 08h(level = 1.0)
Bit [3:2]	SCONR[1:0]	02h	R/W	R Data Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0.75) to 0x0F(level = 1.125) Default value 08h(level = 1.0)

R0C: R Sub-Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit [7:6]	-	-	-	Reserve
Bit [5:0]	SBRIR[5:0]	20h	R/W	R Data Brightness level adjustment register. (1/Step) Adjust range from 0x00(level = -32) to 0x3F(level = +31) Default value 20h(level = 0)

R0D: B Sub-Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit [7:6]	-	-	-	Reserve
Bit [5:0]	SBRIB[5:0]	20h	R/W	B Data Brightness level adjustment register. (1/Step) Adjust range from 0x00(level = -32) to 0x3F(level = +31) Default value 20h(level = 0)

R0E: VCOMDC Level Control Register

Bit	Name	Initial	R/W	Description
Bit [7]	-	-	-	Reserve
Bit [6]	OTP_BYPS	0h	R/W	VCDCSL[5:0] data source selection register OTP_BYPS ="0", VCDCSL[5:0] is read from OTP memory. OTP_BYPS ="1", VCDCSL[5:0] is switch to the 3-wire register memory when user want to adjust the VCOMDC level for test propose. Refer to the "TRMEN" control register for the proper OTP write operation.
Bit [5:0]	VCDCSL [5:0]	10h	R/W	VCOMDC level control register (20mV/Step @ VDDA = 5.0V) VCDCSL[5:0] = 00h, VCOMDC = 1.00V VCDCSL[5:0] = 01h, VCOMDC = 1.02V ….. VCDCSL[5:0] = 10h, VCOMDC = 1.32V ….. VCDCSL[5:0] = 3eh, VCOMDC = 2.24V VCDCSL[5:0] = 3fh, VCOMDC = 2.26V

Note： .VCOMDC always keep 1.7V When VPSW = "1" . The OTP value effect in VPSW=0.

R0F VCOMAC Level Control Register

Bit	Name	Initial	R/W	Description
Bit [7:6]	VGLSL	10	R/W	VGLSL level control register VGLSL Level = 1V / Step
Bit [5:4]	VGHSL	10	R/W	VGHSL level control register VGHSL Level = 1V / Step
Bit [3:0]	VCACSL[3:0]	0100	R/W	VCOMAC level control register VCOMAC Level = 0.1V / Step @ VDDA = 5.0V

VCACSL [3:0]

VCSL3	VCSL2	VCSL1	VCSL0	Level (V)
0	0	0	0	4.6
0	0	0	1	4.7
0	0	1	0	4.8
0	0	1	1	4.9
0	1	0	0	5.0 (Default)
0	1	0	1	5.1
0	1	1	0	5.2
0	1	1	1	5.3
1	0	0	0	5.4
1	0	0	1	5.5
1	0	1	0	5.6
1	0	1	1	5.7
1	1	0	0	5.8
1	1	0	1	5.9
1	1	1	0	6.0
1	1	1	1	6.1

Note：When VPSW = “1” .The register can’t be used

VGHSL[5:4]

VGHSL1	VGHSL0	VGH(V)
0	0	12
0	1	13
1	1	14
1	0	15

When VPSW = “1” .The register can’t be used

VGLSL[7:6]

VGLSL1	VGLSL0	VGL(V)
0	0	-7
0	1	-8
1	1	-9
1	0	-10

When VPSW = “1” .The register can’t be used

R10: VGAM2 Level Control Register

Bit	Name	Initial	R/W	Description
Bit [7:5]	-	-	-	Reserve
Bit [4]	GAMEN	0b	R/W	GAMMA adjustment enable control register.(adjustable voltage for V2-V6) GAEN=”0” or VSET = 1, Gamma correction disabled. GAEN=”1” & VSET=”0”, Gamma correction enabled
Bit [3]	-	-	-	Reserve
Bit [2:0]	V2GAM [2:0]	100b	R/W	V2 GAMMA voltage level setting. Function enabled when VSET=”0” Adjust level = 22mV / Step

R11: VGAM3/4 Level Control Register

Bit	Name	Initial	R/W	Description
Bit [7:6]	-	-	-	Reserve
Bit [5:3]	V4GAM [2:0]	100b	R/W	V4 GAMMA voltage level setting. Function enabled when VSET=”0” Adjust level = 22mV / Step
Bit [2:0]	V3GAM [2:0]	100b	R/W	V3 GAMMA voltage level setting. Function enabled when VSET=”0” Adjust level = 22mV / Step

R12: VGAM5/6 Level Control Register

Bit	Name	Initial	R/W	Description
Bit [10:6]	-	-	-	Reserve
Bit [5:3]	V6GAM [2:0]	100b	R/W	V6 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level = 22mV / Step
Bit [2:0]	V5GAM [2:0]	100b	R/W	V5 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level = 22mV / Step

V2GAM/ V3GAM/ V4GAM/ V5GAM./ V6GAM Level Control Register Setting Table

VxGMA2	VxGMA1	VxGMA0	Voltage level	Unit	Note
0	0	0	+88	mV	Refer to the Gamma Table for the default voltage level of V2 ~ V6
0	0	1	+66	mV	
0	1	0	+44	mV	
0	1	1	+22	mV	
1	0	0	+0(Default)	mV	
1	0	1	-22	mV	
1	1	0	-44	mV	
1	1	1	-66	mV	

Note: x = 2, 3, 4, 5, 6

R20: Wide and narrow display mode Control Register

Bit	Name	Initial	R/W	Description
Bit [7:2]	-	-	-	Reserve
Bit [1:0]	WNSEL [1:0]	00b	R/W	Wide and narrow display mode select register

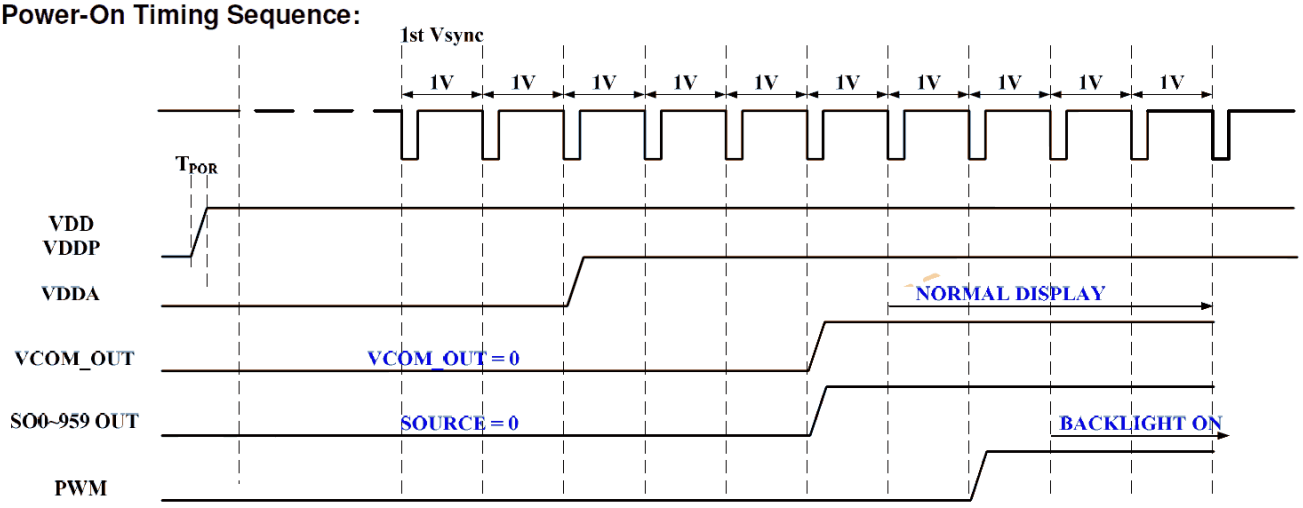
WNSEL[1:0]: Wide and narrow display mode select register

WNSEL1	WNSEL0	Display Mode
0	0	Normal display (Default)
0	1	Narrow display
1	0	Wide display
1	1	234-Line

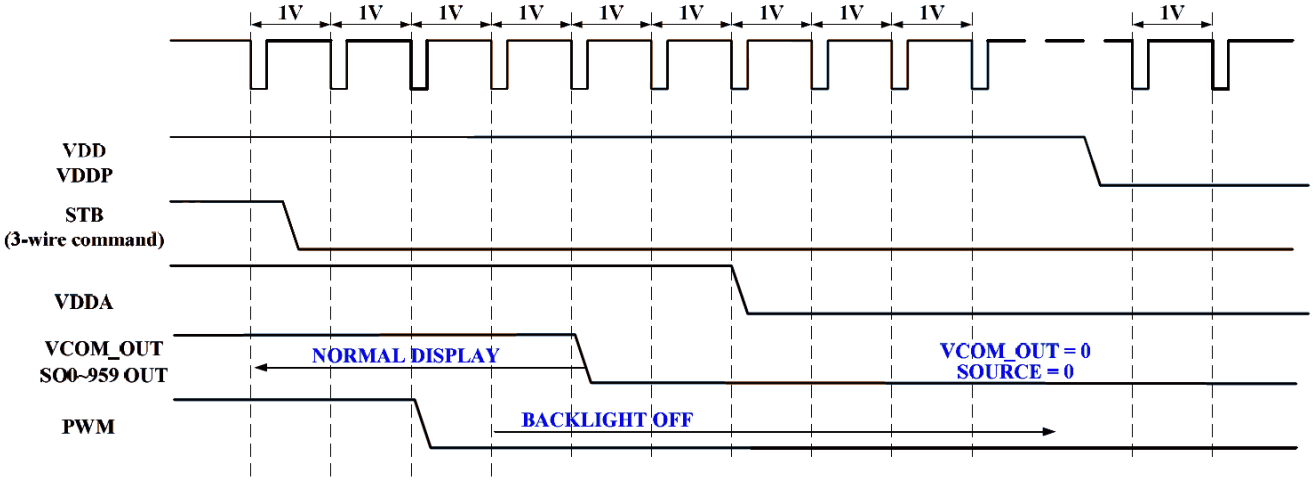
Note: This function will be enabled under CCIR601 and CCIR656 mode

7.4 Power On/Off Sequence

Power-On Timing Sequence:



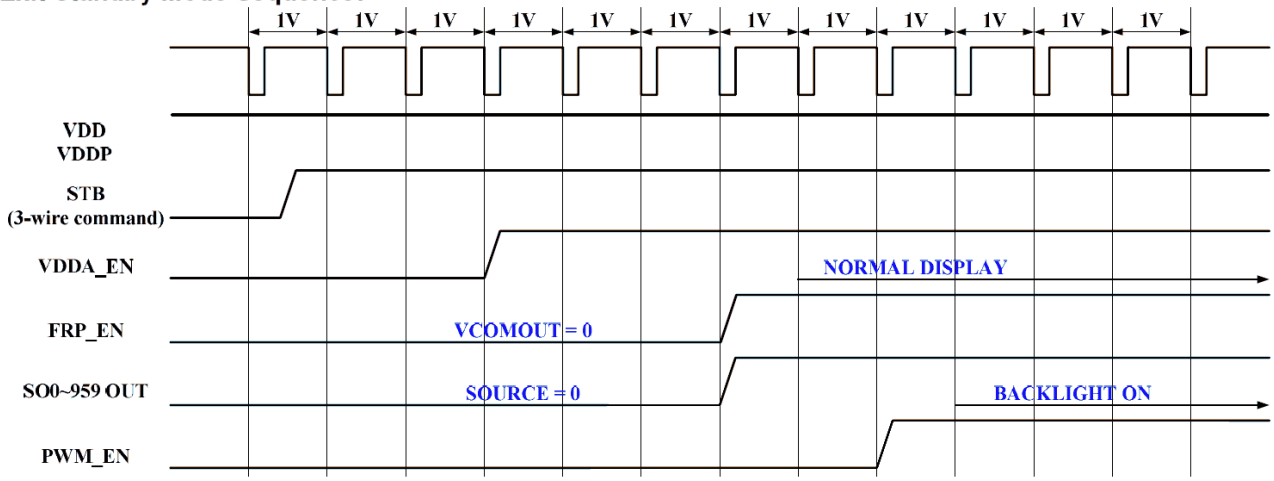
Power-off Timing Sequence:



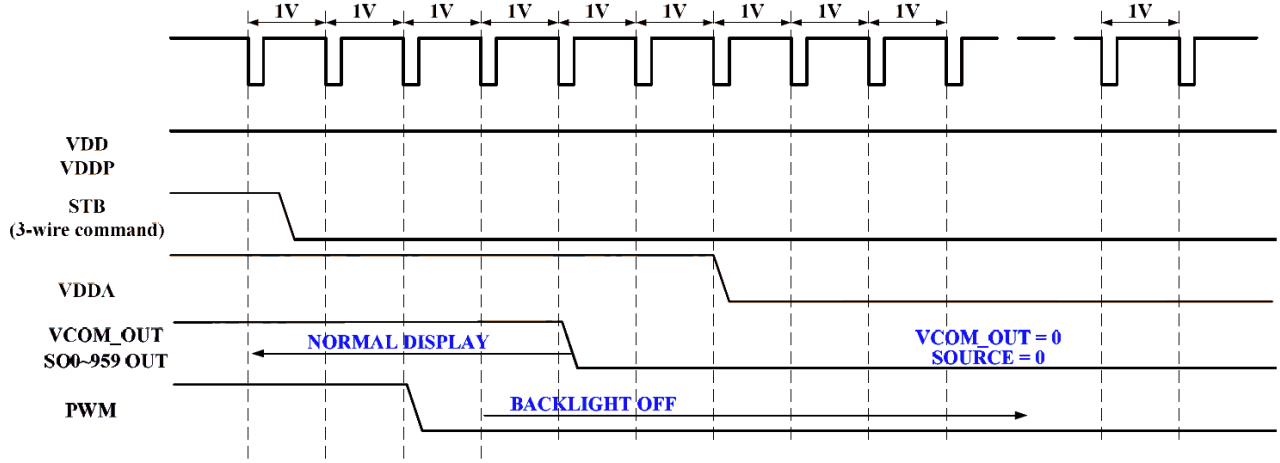
To prevent abnormal display that might show on screen,
it is suggest to use to following standby sequence.
Power on, turn on the backlight AFTER power supply stable and display ready.
Power off, turn off the backlight BEFORE power down.

7.5 Standby Sequence

Exit Standby Mode Sequence:



Entry Standby Mode Sequence:



To prevent abnormal display that might show on screen,
it is suggest to use to following standby sequence.
Entering standby mode, turn off the backlight BEFORE standby.
Exiting standby mode, turn on the backlight AFTER exiting standby mode, power supply stable and display ready.

7.6 Reset Function

To prevent from abnormal reset condition, a glitch filter for RSTB is embedded in this chip. The external reset signal should keep active for large then reset time (T_{RSTB}). Refer to the AC/DC Specification for the requirement.

8. Precautions of using LCD Modules

Mounting

- Mounting must use holes arranged in four corners or four sides.
- The mounting structure so provide even force on to LCD module. Uneven force (ex. Twisted stress) should not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- It is suggested to attach a transparent protective plate to the surface in order to protect the polarizer. It should have sufficient strength in order to the resist external force.
- The housing should adopt radiation structure to satisfy the temperature specification.
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. Never rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics deteriorate the polarizer.)
- When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer

Operating

- The spike noise causes the mis-operation of circuits. It should be within the ±200mV level (Over and under shoot voltage)
- Response time depends on the temperature.(In lower temperature, it becomes longer.)
- Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- When fixed patterns are displayed for a long time, remnant image is likely to occur.
- Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference

Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

Storage

When storing modules as spares for a long time, the following precautions are necessary.

- Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

Protection Film

- When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt tore main on the polarizer. Please carefully peel off the protection film without rubbing it against the polarizer.
- When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

Transportation

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

9. Appendix A <Inspection items and criteria for appearance defect>

Items	Criteria			
Open Segment or Common	Not permitted			
Short	Not permitted			
Wrong Viewing Angle	Not permitted			
Decliners	Not permitted			
Contrast Ration Uneven	According to the limit specimen			
Crosstalk	According to the limit specimen			
White spots	X>1 pixel	A-area	Not permitted	Max 6 spots allowed
		B-area	Max. 1 allowed	
	1/2 pixel<X≤1 pixel	A-area	Not permitted	
		B-area	Max. 2 allowed	
	X≤1/2 pixel	A-area	Max. 1 allowed	
		B-area	Max. 4 allowed	
Black Sport	X>1 pixel	A-area	Not permitted	
		B-area	Max. 2 allowed	
	X≤1/2 pixel	A-area	Max. 1 allowed	
		B-area	Max. 4 allowed	
Line Defect	Apparent vertical horizontal line defects are not permitted			

Note:

1. On Pixel include 3 dots (RedDot + GreenDot + BlueDot)
2. Definition of Panel “A-area” and “B-area”