SONY

Power supply system management & Audio IC

CXD5247GF

Description

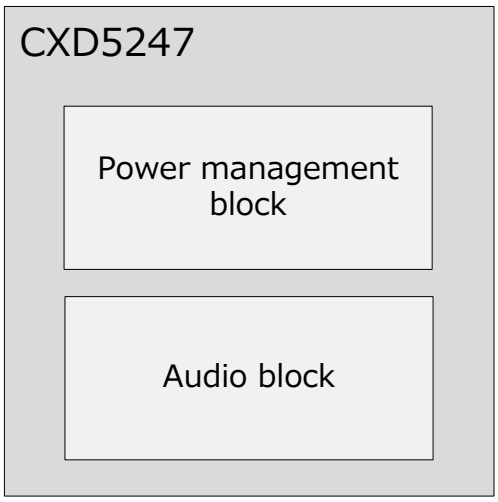
The combination of CXD5247and CXD5602 for high performance wearable applications realizes ideal power supply management with low power consumption.

In addition, CXD5247 also realizes audio input/output functions for the CXD5602 System.

Features

Power management block

◆Low power consumption (RTC block IQ=3 μA typ.)
◆Voltage step down type PFM control DC-DC converter (3ch)
◆LDO (5ch)
◆RTC (32.768 kHz clock output)
◆I2C serial interface
◆GPO (8ch)
◆Load switch : 1.8V(4ch)
◆USB charge function
◆Analog front-end for battery power level detection



Audio block

◆Original data format for CXD5602
◆Amplifier for analog microphone + A/D converter
  ◆Number of channels : 4ch
  ◆PGA setting : 0dB to 24dB, 0.5dB increments
  ◆SNR : 90dB(typ.)
  ◆THD+N : -80dB(typ.)
  ◆Input referred noise : 10uVrms
◆BTL output Class-D amplifier
  ◆Speaker impedance : 8Ω
  ◆THD+N : 54dB
  ◆Noise level : 10uVrms(typ.)
  ◆POP noise reduction function
◆Other functions
  ◆Supported crystals : 24.576MHz/49.152MHz
  ◆GPO(1ch)

Package

XFBGA 156pin

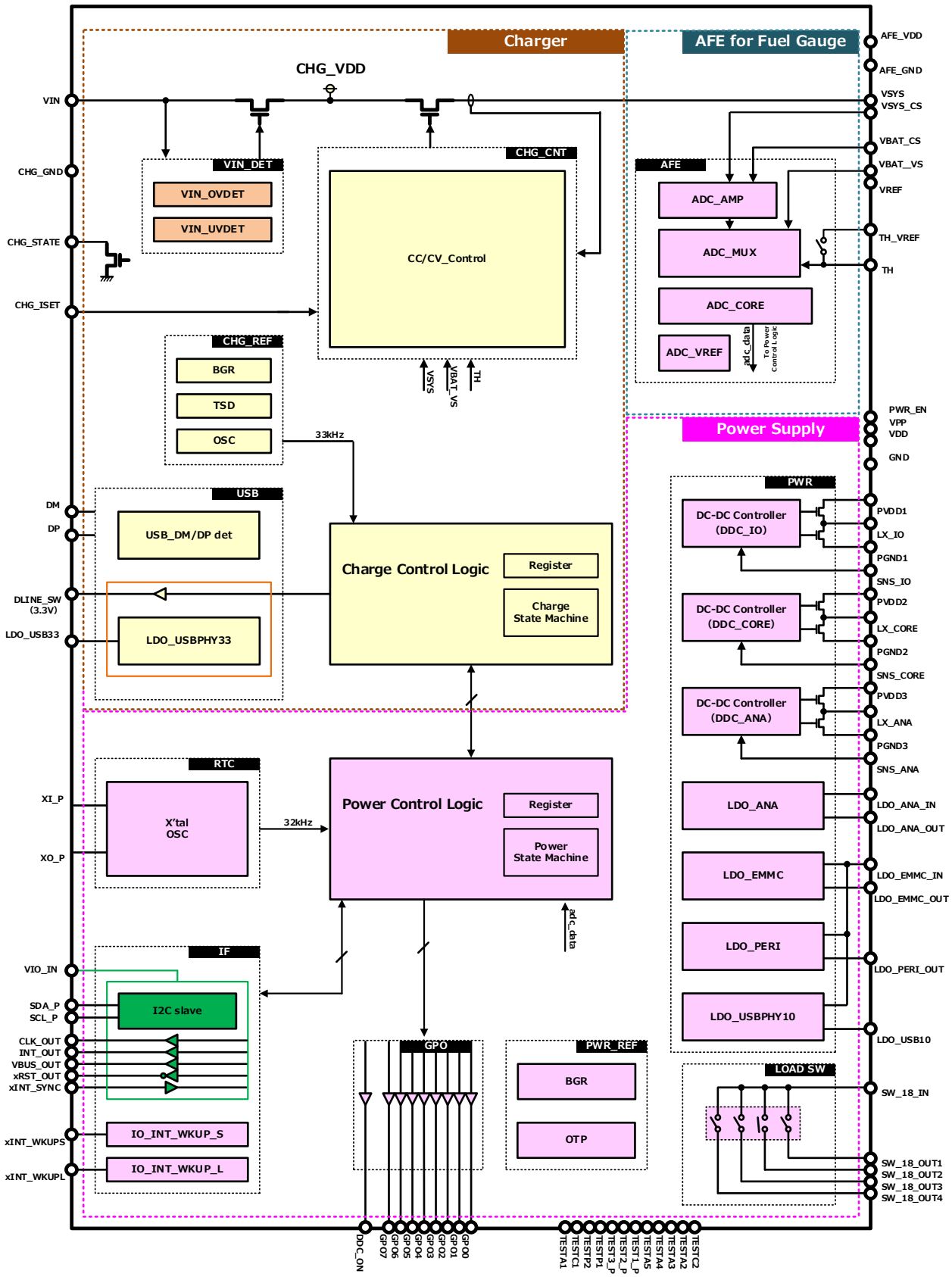
Structure

CMOS Si monolithic IC

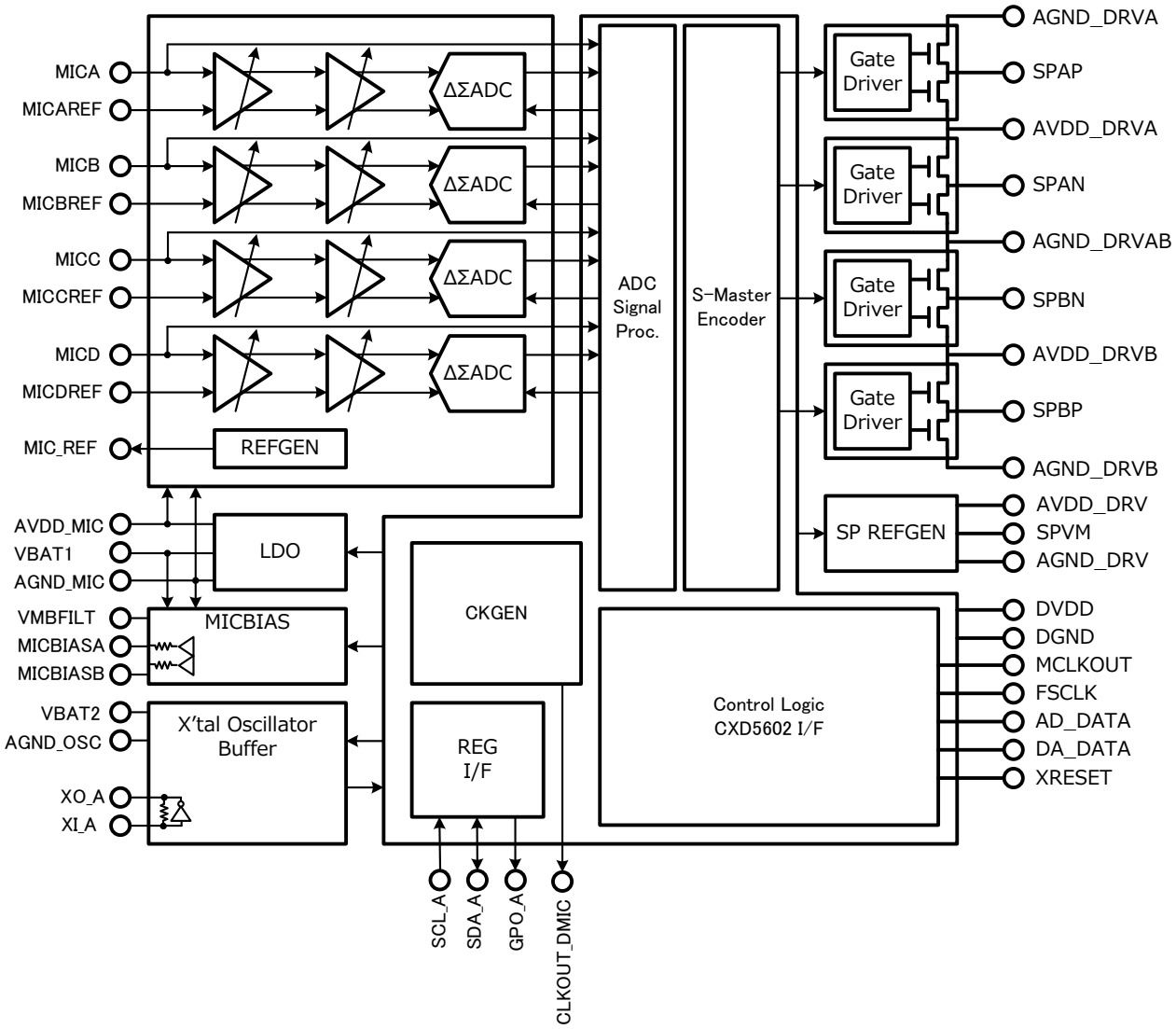
Contents

Block Diagram

◆Power management block

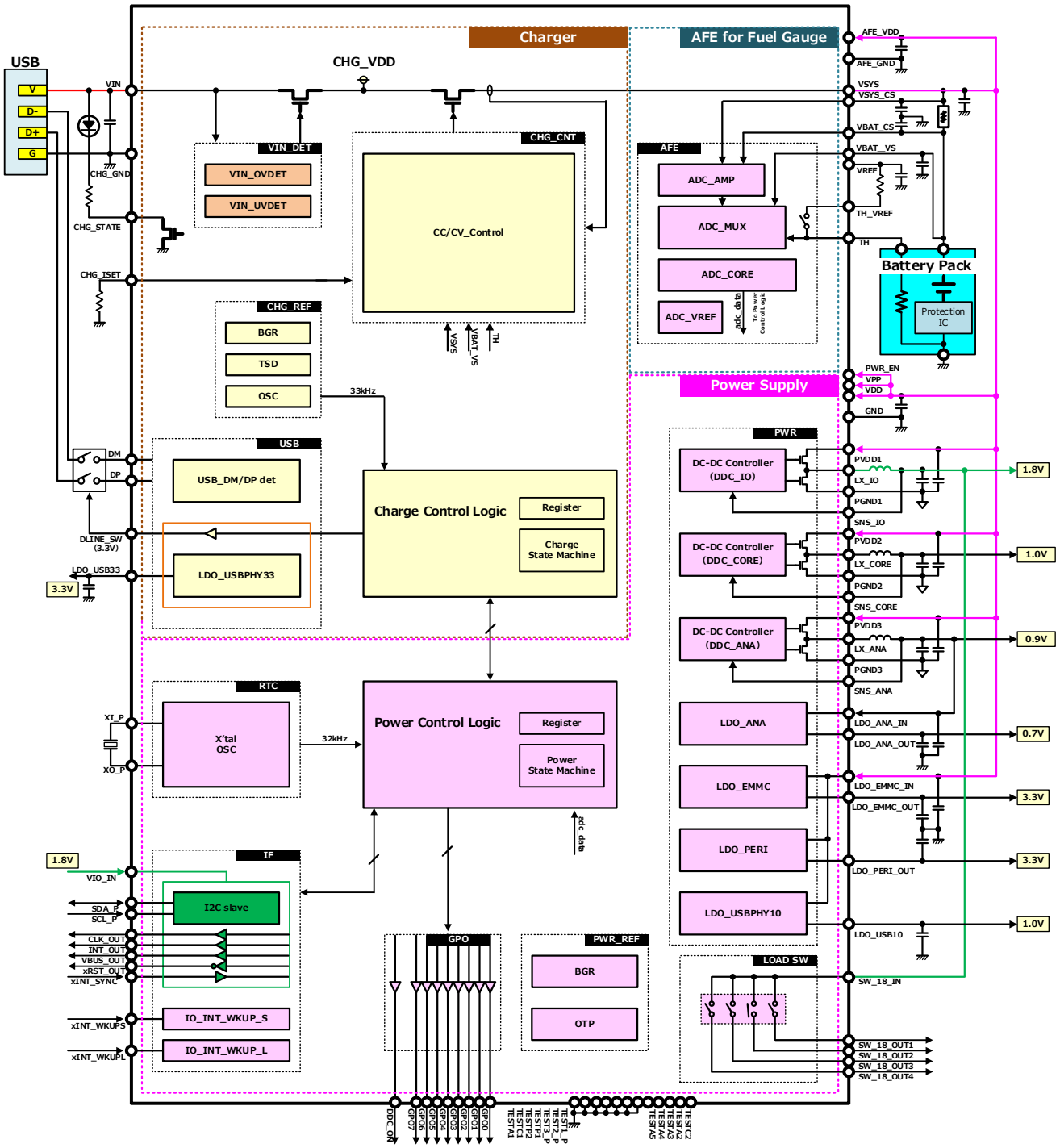


◆Audio Block


MICA
MICAREF
MICB
MICBREF
MICC
MICCREF
MICD
MICDREF
MIC_REF
ΔΣADC
ΔΣADC
ΔΣADC
ΔΣADC
REFGEN
ADC Signal Proc.
S-Master Encoder
Gate Driver
Gate Driver
Gate Driver
Gate Driver
AGND_DRVA
SPAP
AVDD_DRVA
SPAN
AGND_DRVAB
SPBN
AVDD_DRVB
SPBP
AGND_DRVB
SP REFGEN
AVDD_DRV
SPVM
AGND_DRV
AVDD_MIC
VBAT1
AGND_MIC
LDO
VMBFILT
MICBIASA
MICBIASB
MICBIAS
CKGEN
VBAT2
AGND_OSC
X'tal Oscillator Buffer
XO_A
XI_A
REG I/F
Control Logic CXD5602 I/F
DVDD
DGND
MCLKOUT
FSCLK
AD_DATA
DA_DATA
XRESET
SCL_A
SDA_A
GPO_A
CLKOUT_DMIC

Application Circuit

◆Power management block



Power management block (Case : Nonuse of charge function)

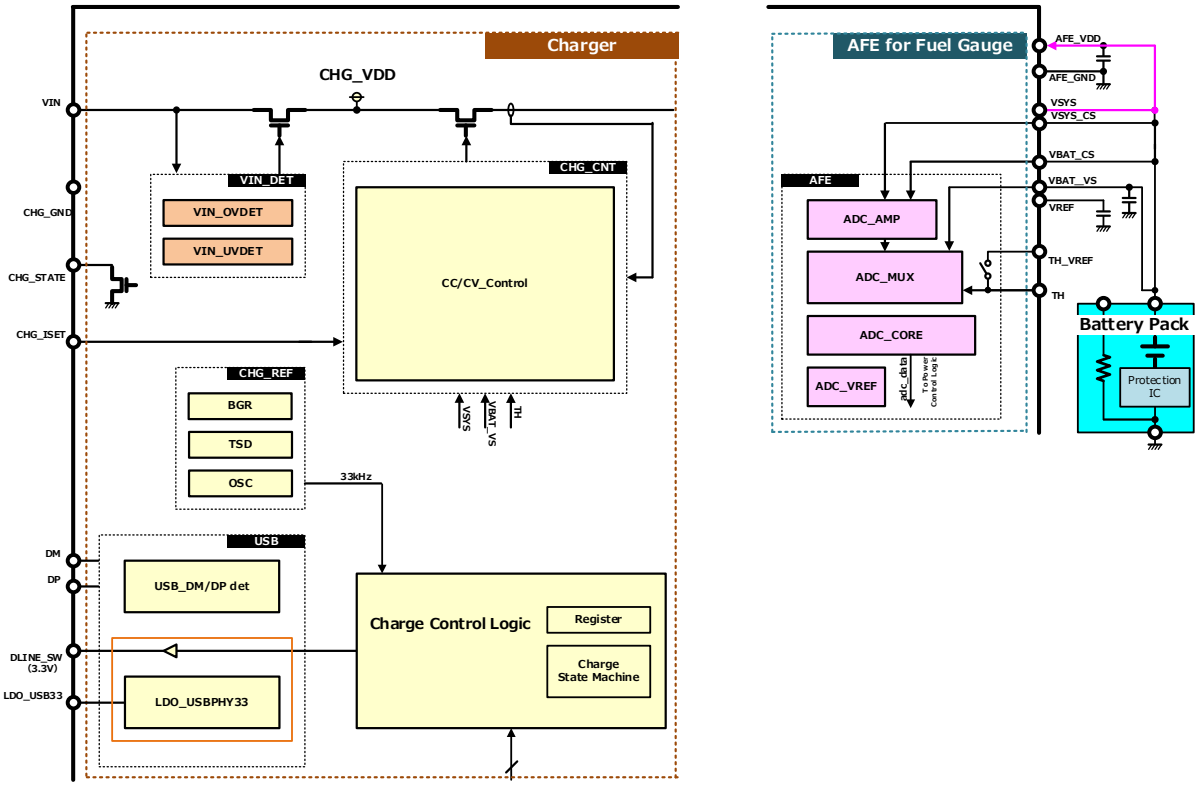
Open-pin : VIN, CHG_STATE, CHG_ISET, DP, DM, DLINE_SW, LDO_USB33

Power management block (Case : Nonuse of fuel gauge function)

Open-pin : TH_VREF, TH

Connect-pin: VSYS, VSYS_CS, VBAT_CS, VBAT_VS, AFE_VDD (VDD)

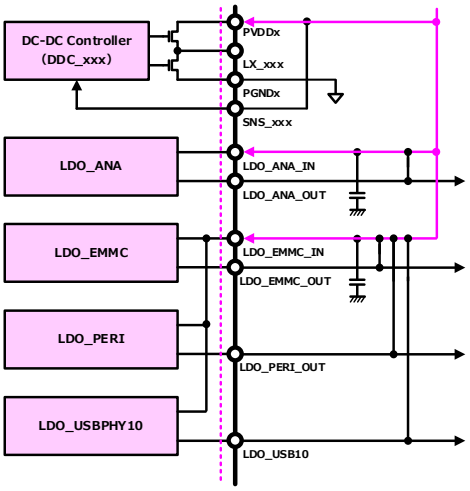
External-part: VREF - 0.22uF, VBAT_VS - 1uF



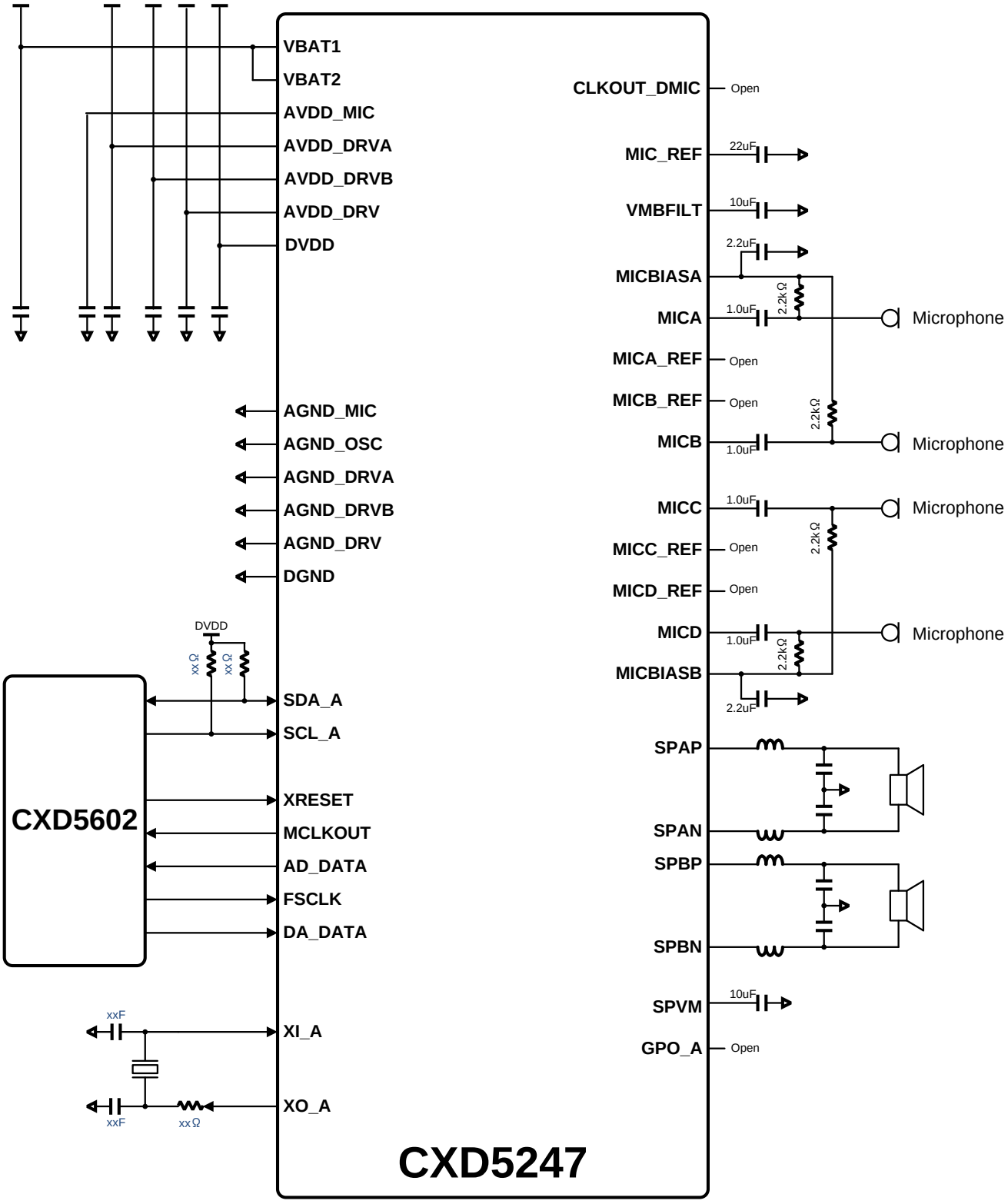
Power management block (Case : Nonuse of power supply)

Open-pin : LX_xxx

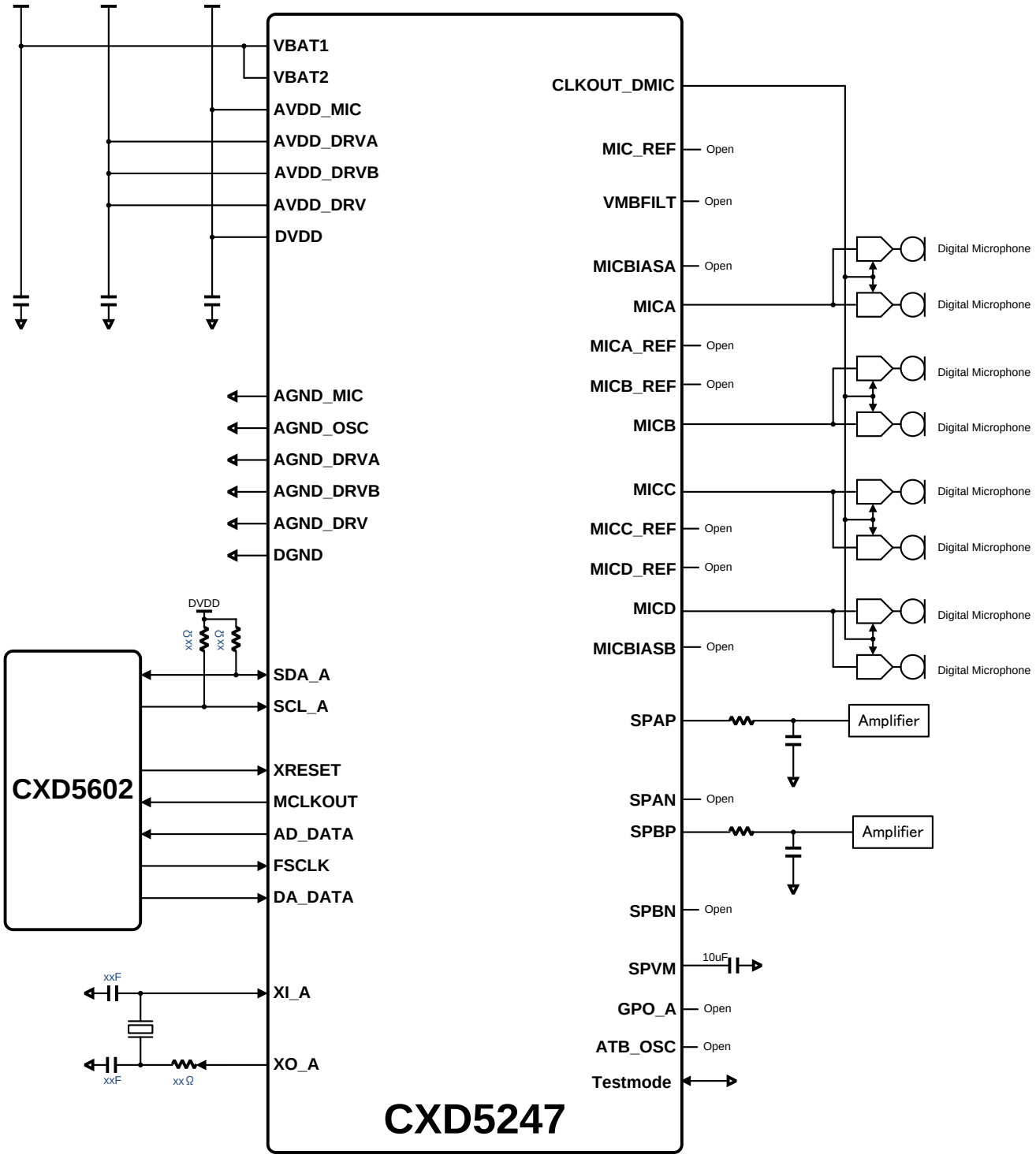
Connect-pin : SNS_xxx to PVDD (VDD), LDO_EMMC_OUT(or PERI_OUT or USB10) to LDO_EMMC_IN



◆**Audio block (Case1：Speaker BTL Drive / 4ch Analog MIC)**



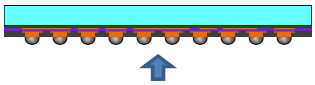
◆Audio block (Cace2：External Speaker Amp / 8ch Digtal MIC)



Pin Configuration

	A	B	C	D	E	F	G	H	J	K	L	M
1	VIN2	VIN4	VSYS2	VSYS4	VREF	AFE_GND	LDO_EMMC_OUT	LDO_EMMC_IN	LDO_PERI_OUT	LDO_USB10	GND1	XI_P
2	VIN1	VIN3	VSYS1	VSYS3	TH_VREF	AFE_VDD	N.C.	N.C.	GND	GND	GND	XO_P
3	DP	CHG_GND1	CHG_GND2	VBAT_VS	TH	N.C.	N.C.	GND	GPO7	GPO6	GPO5	GPO4
4	LDO_USB33	CHG_ISET	DM	CHG_STATE	VBAT_CS	VSYS_CS	N.C.	N.C.	GPO3	GPO2	GPO1	VDD1
5	PVDD2	PVDD2_S	DLINE_SW	GND	N.C.	N.C.	N.C.	N.C.	GPO0	N.C.	GND	LDO_ANA_IN
6	LX_CORE	N.C.	SNS_CORE	N.C.	N.C.	N.C.	GND2	N.C.	xRST_OUT	SNS_ANA	VPP	LDO_ANA_OUT
7	PGND2	PGND2_S	GND3	DDC_ON	GND	DA_DATA	N.C.	N.C.	SDA_P	xINT_SYNC	PGND3_S	PGND3
8	PVDD1	PVDD1_S	PWR_EN	xINT_WKUPL	MCLKOUT	SW_18_OUT2	SW_18_OUT3	N.C.	SCL_P	CLK_OUT	N.C.	LX_ANA
9	LX_IO	N.C.	VDD2	xINT_WKUPS	SW_18_OUT1	SW_18_IN1	SW_18_IN2	SW_18_OUT4	GND4	VBUS_OUT	PVDD3_S	PVDD3
10	PGND1	PGND1_S	SNS_IO	SDA_A	GPO_A	CLKOUT_DMIC	MIC_REF	AGND_MIC	MICDREF	INT_OUT	VIO_IN	GND5
11	XRESET	FSCLK	AD_DATA	SCL_A	GND	MICA	MICB	AVDD_MIC	MICD	MIC BIASB	VMBFILT	SPVM
12	XI_A	AGND_OSC	N.C.	DVDD	DGND	MICAREF	MICBREF	MICC	MICCREF	MIC BIASA	VBAT1	AVDD_DRV
13	XO_A	VBAT2	AGND_DRVA	SPAP	AVDD_DRVA	SPAN	AGND_DRVAB	SPBN	AVDD_DRVB	SPBP	AGND_DRVB	AGND_DRV

Audio	Power



BOTTOM VIEW

Pin Table

No.	Ball #	Ball Name	Power Supply	Type	Description
1	A1	VIN2 (=VIN1)	CHG_GND	Power Supply	Power Supply for USB
2	A2	VIN1	CHG_GND	Power Supply	Power Supply for USB
3	A3	DP	VIN,CHG_GND	Analog	USB bus, D + input
4	A4	LDO_USB33	VIN,CHG_GND	Analog	USB Power Supply LDO 3.3V output
5	A5	PVDD2	PGND2	Power Supply	Power Supply for DDC_core
6	A6	LX_CORE	–	Analog	Switching output for DDC_core
7	A7	PGND2	–	Power Supply	Ground for DDC_core
8	A8	PVDD1	PGND1	Power Supply	Power Supply for DDC_IO
9	A9	LX_IO	–	Analog	Switching output for DDC_IO
10	A10	PGND1	–	Power Supply	Ground for DDC_IO
11	A11	XRESET	DVDD,DGND	Digital INPUT	System Reset
12	A12	XI_A	VBAT2,AGND_OSC	Analog	Crystal Oscillator Input
13	A13	XO_A	VBAT2,AGND_OSC	Analog	Crystal Oscillator Output
14	B1	VIN4 (=VIN1)	CHG_GND	Power Supply	Power Supply for USB
15	B2	VIN3 (=VIN1)	CHG_GND	Power Supply	Power Supply for USB
16	B3	CHG_GND1	–	Power Supply	Ground for Chager
17	B4	CHG_ISET	VIN,CHG_GND	Analog	Charge current setting input
18	B5	PVDD2_S (=PVDD2)	PGND2	Power Supply	Power Supply for DDC_core
19	B6	N.C.	–	–	–
20	B7	PGND2_S (=PGND2)	–	Power Supply	Ground for DDC_core
21	B8	PVDD1_S (=PVDD1)	PGND1	Power Supply	Power Supply for DDC_IO
22	B9	N.C.	–	–	–
23	B10	PGND1_S (=PGND1)	–	Power Supply	Ground for DDC_IO
24	B11	FSCLK	DVDD,DGND	Digital INPUT	Serial Data Frame Clock
25	B12	AGND_OSC	–	Power Supply	Ground for Oscillator
26	B13	VBAT2	AGND_OSC	Power Supply	Power Supply from Battery
27	C1	VSYS2 (=VSYS1)	CHG_GND	Power Supply	Power Supply for SYTEM
28	C2	VSYS1	CHG_GND	Power Supply	Power Supply for SYTEM
29	C3	CHG_GND2 (=CHG_GND1)	–	Power Supply	Ground for Chager
30	C4	DM	VIN,CHG_GND	Analog	USB bus, D - input
31	C5	DLINE_SW	VIN,CHG_GND	Digital OUTPUT	USB bus connection signal
32	C6	SNS_CORE	VDD,GND	Analog	Feedback input for DDC_CORE
33	C7	GND3 (=GND)	–	Power Supply	Ground for PM
34	C8	PWR_EN	VDD,GND	Digital INPUT	Enable input
35	C9	VDD2 (=VDD)	GND	Power Supply	Power Supply for PM

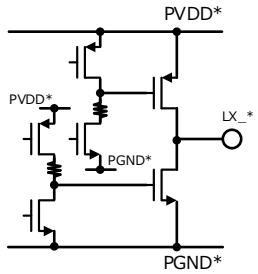
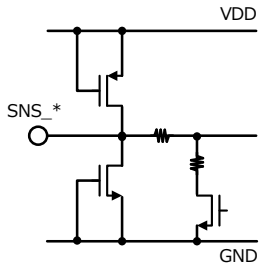
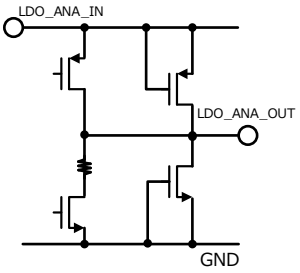
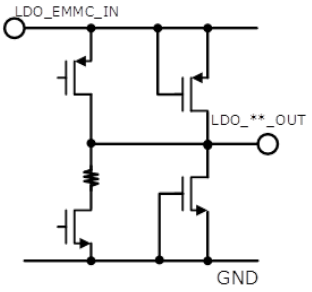
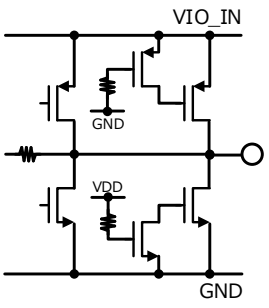
No.	Ball #	Ball Name	Power Supply	Type	Description
36	C10	SNS_IO	VDD,GND	Analog	Feedback input for DDC_IO
37	C11	AD_DATA	DVDD,DGND	Digital OUTPUT	ADC Serial Data Output
38	C12	N.C.	–	–	–
39	C13	AGND_DRVA	–	Power Supply	Ground for Ach Speaker Driver
40	D1	VSYS4 (=VSYS1)	CHG_GND	Power Supply	Power Supply for SYTEM
41	D2	VSYS3 (=VSYS1)	CHG_GND	Power Supply	Power Supply for SYTEM
42	D3	VBAT_VS	CHG_GND	Analog	Battery voltage sense input
43	D4	CHG_STATE	VIN,CHG_GND	Digital OUTPUT	Charge status output
44	D5	GND	–	–	–
45	D6	N.C.	–	–	–
46	D7	DDC_ON	VDD,GND	Digital OUTPUT	DDC_CORE start-up output
47	D8	xINT_WKUPL	VDD,GND	Digital INPUT	Long time interrupt input
48	D9	xINT_WKUPS	VDD,GND	Digital INPUT	Short time interrupt input
49	D10	SDA_A	DVDD,DGND	Digital OUTPUT	I2C Serial Control Data
50	D11	SCL_A	DVDD,DGND	Digital INPUT	I2C Serial Control Port Clock
51	D12	DVDD	DVDD,DGND	Power Supply	Power Supply for 1.8V Digital Domain
52	D13	SPAP	AVDD_DRVA,AGND_DRVA	Analog	Positive Speaker Output of Ach
53	E1	VREF	AFE_VDD,AFE_GND	Analog	VREF output
54	E2	TH_VREF	AFE_VDD,AFE_GND	Analog	Thermistor monitor input
55	E3	TH	AFE_VDD,AFE_GND	Analog	Thermistor input
56	E4	VBAT_CS	CHG_GND	Analog	Battery current sense input
57	E5	N.C.	–	–	–
58	E6	N.C.	–	–	–
59	E7	GND	–	–	–
60	E8	MCLKOUT	DVDD,DGND	Digital OUTPUT	Master Clock Output
61	E9	SW_18_OUT1	SW_18_IN,GND	Analog	Load switch output (for USB)
62	E10	GPO_A	DVDD,DGND	Digital OUTPUT	General Purpose Output
63	E11	GND	–	–	–
64	E12	DGND (=GND)	–	Power Supply	Ground for 1.8V Digital Domain
65	E13	AVDD_DRVA	AGND_DRVA	Power Supply	Power Supply for Ach Speaker Driver
66	F1	AFE_GND	–	Power Supply	Ground for AFE
67	F2	AFE_VDD	AFE_GND	Power Supply	Power Supply for AFE
68	F3	N.C.	–	–	–
69	F4	VSYS_CS	VSYS,CHG_GND	Analog	VSYS current sense input
70	F5	N.C.	–	–	–
71	F6	N.C.	–	–	–
72	F7	DA_DATA	DVDD,DGND	Digital INPUT	DAC Serial Data Input

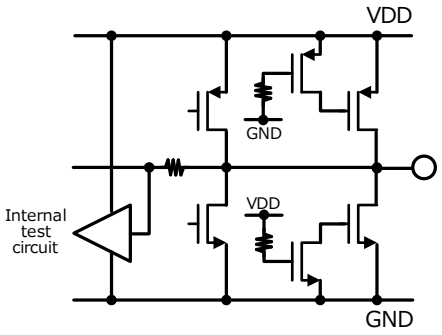
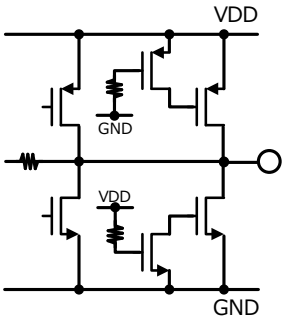
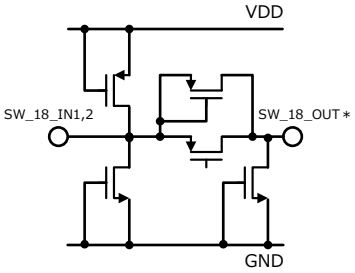
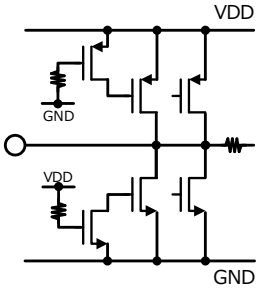
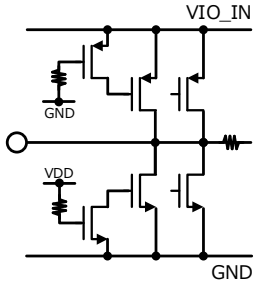
No.	Ball #	Ball Name	Power Supply	Type	Description
73	F8	SW_18_OUT2	SW_18_IN,GND	Analog	Load switch output
74	F9	SW_18_IN1	VDD,GND	Analog	Load switch input
75	F10	CLKOUT_DMIC	DVDD,DGND	Digital OUTPUT	Clock Output for Digital Microphone
76	F11	MICA	AVDD_MIC,AGND_MIC	Analog	Microphone Input
77	F12	MICAREF	AVDD_MIC,AGND_MIC	Analog	Reference terminal for Microphone Input
78	F13	SPAN	AVDD_DRVA,AGND_DRVA	Analog	Negative Speaker Output of Ach
79	G1	LDO_EMMC_OUT	LDO_EMMC_IN,GND	Analog	Power supply LDO output for EMMC
80	G2	N.C.	–	–	–
81	G3	N.C.	–	–	–
82	G4	N.C.	–	–	–
83	G5	N.C.	–	–	–
84	G6	GND2 (=GND)	–	Power Supply	Ground for PM
85	G7	N.C.	–	–	–
86	G8	SW_18_OUT3	SW_18_IN,GND	Analog	Load switch output
87	G9	SW_18_IN2 (=SW_18_IN1)	VDD,GND	Analog	Load switch input
88	G10	MIC_REF	AVDD_MIC,AGND_MIC	Analog	Common Reference for MIC ADC
89	G11	MICB	AVDD_MIC,AGND_MIC	Analog	Microphone Input
90	G12	MICBREF	AVDD_MIC,AGND_MIC	Analog	Reference terminal for Microphone Input
91	G13	AGND_DRVAB	–	Power Supply	Ground for Ach/Bch Speaker Driver
92	H1	LDO_EMMC_IN	GND	Analog	Power supply LDO input for EMMC
93	H2	N.C.	–	–	–
94	H3	GND	–	–	–
95	H4	N.C.	–	–	–
96	H5	N.C.	–	–	–
97	H6	N.C.	–	–	–
98	H7	N.C.	–	–	–
99	H8	N.C.	–	–	–
100	H9	SW_18_OUT4	SW_18_IN,GND	Analog	Load switch output
101	H10	AGND_MIC	–	Power Supply	Ground for MIC Input and MIC bias
102	H11	AVDD_MIC	AGND_MIC	Power Supply	Power Supply for Microphone Input
103	H12	MICC	AVDD_MIC,AGND_MIC	Analog	Microphone Input
104	H13	SPBN	AVDD_DRVB,AGND_DRVB	Analog	Negative Speaker Output of Bch
105	J1	LDO_PERI_OUT	LDO_EMMC_IN,GND	Analog	Power supply LDO output for peripheral equipment
106	J2	GND	–	–	–
107	J3	GPO7	VDD,GND	Digital OUTPUT	General-purpose output
108	J4	GPO3	VDD,GND	Digital OUTPUT	General-purpose output
109	J5	GPO0	VDD,GND	Digital OUTPUT	General-purpose output

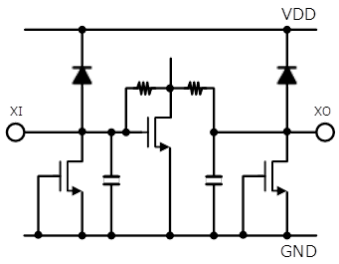
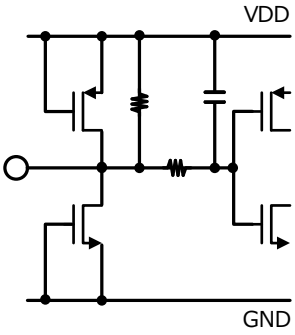
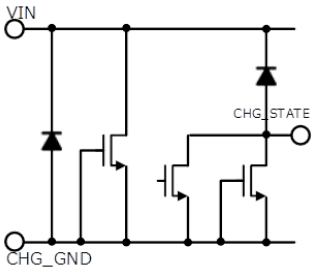
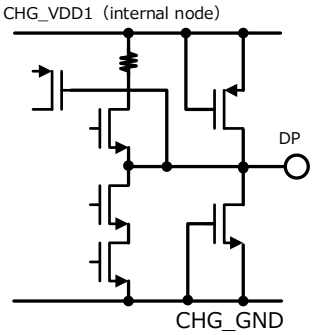
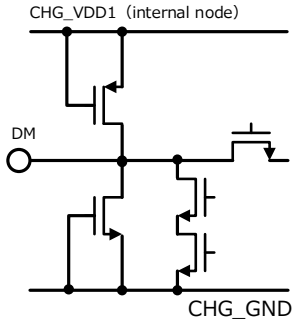
No.	Ball #	Ball Name	Power Supply	Type	Description
110	J6	xRST_OUT	VIO_IN,GND	Digital OUTPUT	Reset output
111	J7	SDA_P	VIO_IN,GND	Digital INPUT	Serial data input
112	J8	SCL_P	VIO_IN,GND	Digital INPUT	Serial clock input
113	J9	GND4 (=GND)	—	Power Supply	Ground for PM
114	J10	MICDREF	AVDD_MIC,AGND_MIC	Analog	Reference terminal for Microphone Input
115	J11	MICD	AVDD_MIC,AGND_MIC	Analog	Microphone Input
116	J12	MICCREF	AVDD_MIC,AGND_MIC	Analog	Reference terminal for Microphone Input
117	J13	AVDD_DRVB	AGND_DRVB	Power Supply	Power Supply for Bch Speaker Driver
118	K1	LDO_USB10	LDO_EMMC_IN,GND	Analog	Power supply LDO output for USB
119	K2	GND	—	—	—
120	K3	GPO6	VDD,GND	Digital OUTPUT	General-purpose output
121	K4	GPO2	VDD,GND	Digital OUTPUT	General-purpose output
122	K5	N.C.	—	—	—
123	K6	SNS_ANA	VDD,GND	Analog	Feedback input for DDC_ANA
124	K7	xINT_SYNC	VIO_IN,GND	Digital INPUT	Interrupt input for time synchronization
125	K8	CLK_OUT	VIO_IN,GND	Digital OUTPUT	Clock output
126	K9	VBUS_OUT	VIO_IN,GND	Digital OUTPUT	USB connection detection output
127	K10	INT_OUT	VIO_IN,GND	Digital OUTPUT	Interrupt output
128	K11	MICBIASB	VBAT1,AGND_MIC	Analog	Microphone Bias
129	K12	MICBIASA	VBAT1,AGND_MIC	Analog	Microphone Bias
130	K13	SPBP	AVDD_DRVB,AGND_DRVB	Analog	Positive Speaker Output of Bch
131	L1	GND1 (=GND)	—	Power Supply	Ground for PM
132	L2	GND	—	—	—
133	L3	GPO5	VDD,GND	Digital OUTPUT	General-purpose output
134	L4	GPO1	VDD,GND	Digital OUTPUT	General-purpose output
135	L5	GND	—	—	—
136	L6	VPP	GND	Analog	Power supply for OTP write
137	L7	PGND3_S (=PGND3)	—	Power Supply	Ground for DDC_ANA
138	L8	N.C.	—	—	—
139	L9	PVDD3_S (=PVDD3)	PGND1	Power Supply	Power Supply for DDC_ANA
140	L10	VIO_IN	GND	Power Supply	Power Supply for IO
141	L11	VMBFILT	VBAT1,AGND_MIC	Analog	Bias voltage of Microphone Bias
142	L12	VBAT1	VBAT1,AGND_MIC	Power Supply	Power Supply from Battery
143	L13	AGND_DRVB	—	Power Supply	Ground for Bch Speaker Driver
144	M1	XI_P	VDD,GND	Analog	Crystal input
145	M2	XO_P	VDD,GND	Analog	Crystal output
146	M3	GPO4	VDD,GND	Digital OUTPUT	General-purpose output

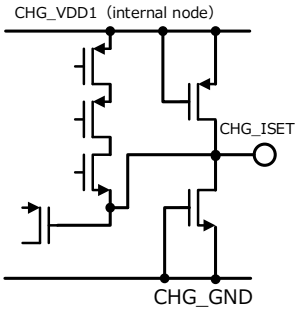
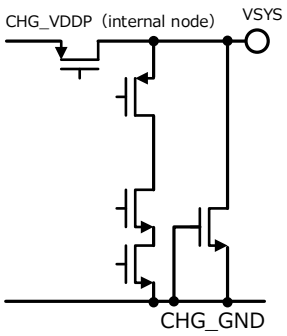
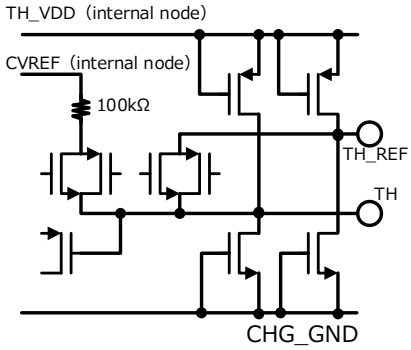
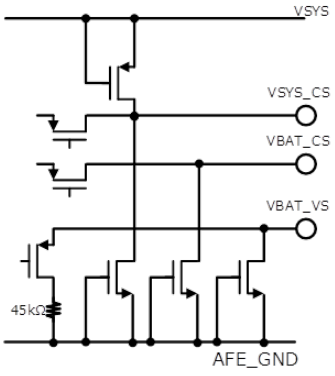
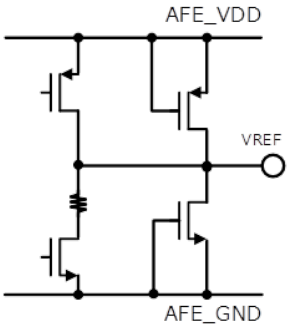
No.	Ball #	Ball Name	Power Supply	Type	Description
147	M4	VDD1 (=VDD)	GND	Power Supply	Power Supply for PM
148	M5	LDO_ANA_IN	GND	Analog	Power supply LDO input for Analog Core
149	M6	LDO_ANA_OUT	LDO_ANA_IN,GND	Analog	Power supply LDO output for Analog Core
150	M7	PGND3	—	Power Supply	Ground for DDC_ANA
151	M8	LX_ANA	—	Analog	Switching output for DDC_ANA
152	M9	PVDD3	PGND1	Power Supply	Power Supply for DDC_ANA
153	M10	GND5 (=GND)	—	Power Supply	Ground for Digital
154	M11	SPVM	AVDD_DRV,AGND_DRV	Analog	Reference for Speaker Driver
155	M12	AVDD_DRV	AGND_DRV	Power Supply	Power Supply for Driver Analog circuits
156	M13	AGND_DRV	—	Power Supply	Ground for Driver Analog circuits

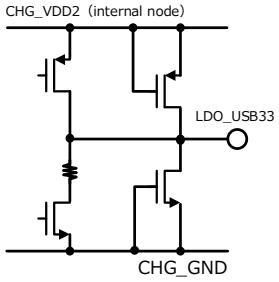
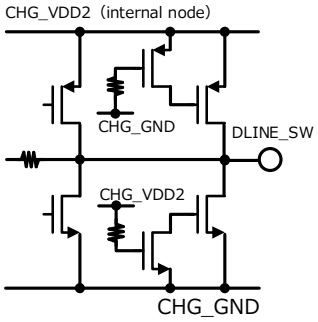
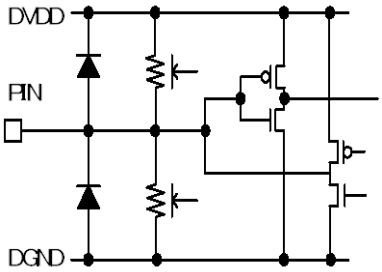
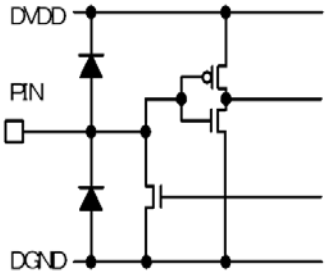
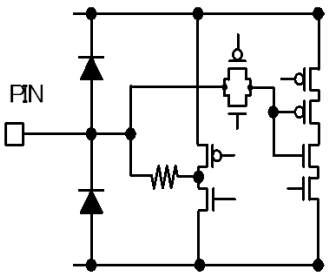
Pin Description

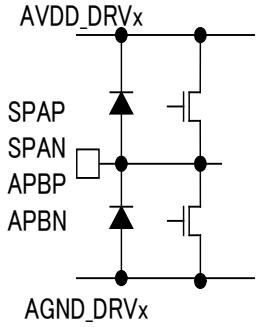
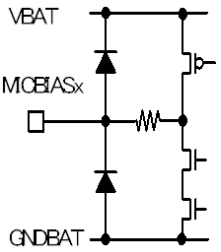
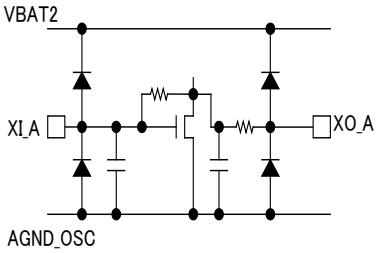
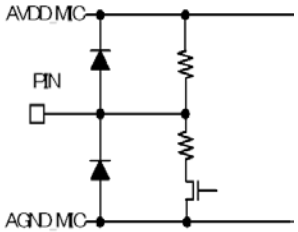
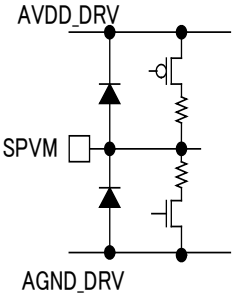
Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
A9,B9 A6,B6 M8,L8	LX_IO LX_CORE LX_ANA	O	PVDD1～PGND1 PVDD2～PGND2 PVDD3～PGND3	
C10 C6 K6	SNS_IO SNS_CORE SNS_ANA	I	1.8V 1.0V 0.9V	
M5 M6	LDO_ANA_IN LDO_ANA_OUT	I O	VDD～GND 3.3V	
H1 G1 J1 K1	LDO_EMMC_IN LDO_EMMC_OUT LDO_PERI_OUT LDO_USB10	I O O O	VDD～GND 3.3V 3.3V 1.0V	
K10 K8 J6 K9	INT_OUT CLK_OUT xRST_OUT VBUS_OUT	O	GND/VIO_IN	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
J5 L4 K4 J4 M3 L3 K3 J3	GPO0 GPO1 GPO2 GPO3 GPO4 GPO5 GPO6 GPO7	O	GND/VDD	 Caution Be sure to pull up or pull down the GPO pin.
D7	DDC_ON	O	GND/VDD	
F9 G9 E9 F8 G8 H9	SW_18_IN1 SW_18_IN2 SW_18_OUT1 SW_18_OUT2 SW_18_OUT3 SW_18_OUT4	I I O O O O	1.8V～GND 1.8V～GND SW_18_IN1,2 SW_18_IN1,2 SW_18_IN1,2 SW_18_IN1,2	
C8	PWR_EN	I	VDD～GND	
J7 J8 K7	SDA_P SCL_P xINT_SYNC	I/O I I	VIO_IN～GND VIO_IN～GND VIO_IN～GND	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
M1 M2	XI_P XO_P	I O	VDD～GND VDD～GND	
D9 D8	xINT_WKUPS xINT_WKUPL	I I	VDD～GND VDD～GND	
D4	CHG_STATE	O	VIN～CHG_GND	
A3	DP	O	0.6V	
C4	DM	I	0～0.6V	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
B4	CHG_ISET	O	0～1.3V	
C1 C2 C3 C4	VSYS	O	0～4.2V	
E2 E3	TH_REF TH	I I	0.6V 0.6V	
F4 E4 D3	VSYS_CS VBAT_CS VBAT_VS	I I I	0～4.2V 0～4.2V 0～4.2V	
E1	VREF	O	2.0V	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
A4	LDO_USB33	O	3.3V	
C5	DLINE_SW	O	0V/ 3.3V	
F10 C11 F7 B11 E8 A11 E10	CLKOUT_DMC, AD_DATA, DA_DATA, FSCLK, MCLKOUT, XRESET, GPO_A	O O I I O I O	0V/1.8V	
D10 D11	SDA_A SCL_A	I/O I	0V/1.8V	
F11 G11 H12 J11	MICA MICB MICC MICD	I	0.9V±0.225V	

Pin No.	Symbol	I/O	Standard pin voltage	Equivalent circuit
D13 F13 K13 H13	SPAP SPAN SPBP SPBN	O	0V/3.3V	
K12 K11 L11	MICBIASA MICBIASB VMBFILT	O	2V	
A12 A13	XI_A XO_A	I O	0V/1.8V	
F12 G12 J12 J10 G10	MICAREF MICBREF MICCREF MICDREF MIC_REF	OI	0.9V	
M11	SPVM	O	1.65V	

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remarks
Maximum input voltage (Power)	V_{IN_MAX}	16.0	V	VIN*, CHG_STATE
Power supply (Power)	V_{VDD_MAX}	7.0	V	VSYS*,VDD*,PVDD*,AFE_VDD,VIO_IN
Power supply (Audio)	V_{BAT_MAX}	5.5	V	VBAT*,AVDD_DRV*
	V_{DVDD_MAX}	2.0	V	DVDD,AVDD_MIC
I/O pin voltage 1 (Power)	V_{IO1}	-0.3～VDD+0.3	V	Except for maximum input voltage, Power Supply, I/O pin voltage 2~4, and output pins
I/O pin voltage 2 (Power)	V_{IO2}	-0.3～VIO_IN+0.3	V	xRST_OUT, CLK_OUT, INT_OUT, SDA_P, SCL_P, VBUS_OUT
I/O pin voltage 3 (Audio)	V_{IO3}	-0.3～DBAT*+0.3	V	SPAP,SPAN,SPBP,SPBN,MICBIASA,MICBIASB, VMBFILT,XI_A,XO_A,SPVM
I/O pin voltage 4 (Audio)	V_{IO4}	-0.3～DVDD+0.3	V	SDA_A,SCL_A,XRESET,MCLKOUT,AD_DATA, FSCLK,DA_DATA,,CLKOUT_DMIC,GPO_A, MIC_REF,,MICA,MICB,MICC,MICD,MICAREF, MICBREF,MICCREF,MICDREF,
Maximum junction temperature	T_{j_max}	+ 125	℃	
Storage temperature	T_{stg}	-65 ~ +150	℃	

Recommended Operating Conditions

Item	Symbol	Rating	Unit	Remarks
Ambient operating temperature	Ta	-25 ~ +85	℃	
Supply voltage range 1	VIN	4.5 ~ 5.5	V	VIN*
Supply voltage range 2	VSYS	2.5 ~ 4.4	V	VSYS*,VDD*, PVDD*, AFE_VDD
Supply voltage range 3	VIO_IN	1.62 ～ 1.98	V	VIO_IN
Supply voltage range 4	DVDD	1.62 ～ 1.98	V	DVDD,AVDD_MIC
Supply voltage range 5	AVDD_DRV	3.0 ～ 3.6	V	AVDD_DRV*
Supply voltage range 6	VBAT	2.5 ～ 5.5	V	VBAT*
DC-DC converter output inductor	Lo1	2.2	µH	DDC_IO, DDC_CORE VLS2010ET-2R2M(TDK)
	Lo2	10	µH	DDC_ANA VLS2010ET-100M(TDK)
DC-DC converter output capacitance	Co_DDC1	22*2 parallel connection	µF	DDC_IO, DDC_CORE AMK107BBJ226MA-T (Taiyo Yuden Co., Ltd.)
	Co_DDC2	22	µF	DDC_ANA AMK107BBJ226MA-T(Taiyo Yuden Co., Ltd.)
LDO output capacitance	Co_LDO1	1	µF	LDO_USB33, LDO_USB10, LDO_PERI_OUT
	Co_LDO2	10	µF	LDO_EMMC_OUT
	Co_LDO3	22	µF	LDO_ANA_OUT
VREF output capacitance	Co_VREF	0.22	µF	VREF
VBAT capacitance	Co_VBAT	1	µF	VBAT
VSYS output capacitance	Co_VSYS	1	µF	VSYS
VSYS line total capacitance	C_VSYSALL	10~100	µF	Total including the VDD and PVDD line input capacitance (effective capacitance)
Crystal oscillation frequency	f_{XT}	32.768	kHz	NX3215SA(NDK), TFX-04(RIVER ELETEC) The capacity in the CHIP is 9.5pF (Typ). The CL level of the crystal assumes a thing of 5.0-6.0pF. 32768 Hz crystal is allowed 55kohm max ESR.
Current sense resistor	Rimon	100	mohm	Set as Ichgmax*Rimon≒50mV
Lithium ion battery capacity	Li-ion_cap	~500	mAh	
Rapid charge current	Ichg_set	100~500	mA	Riset=100~20kohm
Thermistor resistance B constant		4250	K	NCP15WF104F03RC (Murata Manufacturing Co., Ltd.)

Electrical Characteristics

◆Power supply Block

(Unless otherwise specified: Ta = 27 °C, VDD = PVDD1 = PVDD2 =PWR_EN = 3.6 V, VIO_IN = SW_IN = 1.8 V)

Power supply input (VDD, VIO_IN)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Power consumption in VDD operating state	I_{VDD1}	Power ON state, No Switching		60		µA
Power consumption in VDD stop state	I_{VDD2}	PWR_EN = 0V			1	µA
Power consumption in VDD Deep Sleep state	I_{VDD3}	VDD=3.6, Deep Sleep state , VIO_IN=OPEN		2	5	µA
Power consumption in VIO_IN operating state	I_{VIO1}	I2C operation state		3		uA
Power consumption in VIO_IN stop state	I_{VIO2}	I2C stop state (SDA_P and SCL_P pulled up)			0.1	uA
UVLO detection voltage	V_{UVLO_L}		2.40	2.45	2.50	V
UVLO cancel voltage	V_{UVLO_H}		2.50	2.55	2.60	V
UVLO hysteresis width	$\triangle V_{UVLO}$	$\triangle V_{UVLO} = V_{UVLO\_H} - V_{UVLO\_L}$	-	100	-	mV

RTC (XI_P, XO_P)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Crystal oscillation frequency	f_{XT}			32.768		kHz
CLK_OUT output Duty	X_{duty}	* Design guarantee item	10		90	%

LOAD SW (SW_18_IN, SW_18_OUT1-4)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
ON resistor 1 (exclusively for USB-PHY)	R_{ON_SW}	I_{SW} = 50mA; SW_18_IN = 1.75V, SW_18_OUT1	-	0.8	1	Ω
ON resistor 2	R_{ON_SW}	I_{SW} = 50mA; SW_18_IN = 1.75V, SW_18_OUT2~4	-	0.8	1	Ω

IF-IN (PWR_EN, xINT_WKUP_S, xINT_WKUP_L, xINT_SYNC, SCL_P, SDA_P)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PWR_EN pin H level input voltage	V_{IPE_H}		VDD − 0.3	-	-	V
PWR_EN pin L level input voltage	V_{IPE_L}		-	-	0.3	V
xINT_WKUP pin H level input voltage	$V_{IxINT\_WKUP\_H}$		VDD − 0.3	-	-	V
xINT_WKUP pin L level input voltage	$V_{IxINT\_WKUP\_L}$		-	-	0.3	V
xINT_SYNC pin H level input voltage	$V_{IxINT\_SYNC\_H}$		VIO_IN − 0.3	-	-	V
xINT_SYNC pin L level input voltage	$V_{IxINT\_SYNC\_L}$		-	-	0.3	V
SCL_P pin H level input voltage	$V_{ISCL\_P\_H}$		VIO_IN − 0.3	-	-	V
SCL_P pin L level input voltage	$V_{ISCL\_P\_L}$		-	-	0.3	V
SDA_P pin H level input voltage	$V_{ISDA\_P\_H}$		VIO_IN − 0.3	-	-	V
SDA_P pin L level input voltage	$V_{ISDA\_P\_L}$		-	-	0.3	V

IF-OUT (CLK_OUT, INT_OUT, xRST_OUT, VBUS_OUT, GPO0-7, DDC_ON)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
CLK_OUT pin H level output voltage	$V_{OCLK\_OUT\_H}$	I_{OUT} =-2mA	VIO_IN – 0.2V	-	-	V
CLK_OUT pin L level output voltage	$V_{OCLK\_OUT\_L}$	I_{IN} =+2mA	-	-	0.2	V
INT_OUT pin H level output voltage	$V_{OINT\_OUT\_H}$	I_{OUT} =-2mA	VIO_IN – 0.2V	-	-	V
INT_OUT pin L level output voltage	$V_{OINT\_OUT\_L}$	I_{IN} =+2mA	-	-	0.2	V
xRST_OUT pin H level output voltage	$V_{OxRST\_OUT\_H}$	I_{OUT} =-2mA	VIO_IN – 0.2V	-	-	V
xRST_OUT pin L level output voltage	$V_{OxRST\_OUT\_L}$	I_{IN} =+2mA	-	-	0.2	V
VBUS_OUT pin H level output voltage	$V_{OVBUS\_OUT\_H}$	I_{OUT} =-2mA	VIO_IN – 0.2V	-	-	V
VBUS_OUT pin L level output voltage	$V_{OVBUS\_OUT\_L}$	I_{IN} =+2mA	-	-	0.2	V
GPO0~7 pin H level output voltage	V_{OGPO1_H}	I_{OUT} =-2mA	VDD – 0.2V	-	-	V
GPO0~7 pin L level output voltage	V_{OGPO1_L}	I_{IN} =+2mA	-	-	0.2	V
DDC_ON pin H level output voltage	$V_{DDC\_ON\_H}$	I_{OUT} =-2mA	VDD – 0.2V	-	-	V
DDC_ON pin L level output voltage	$V_{DDC\_ON\_L}$	I_{IN} =+2mA	-	-	0.2	V

DDC_IO

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Maximum output current[*1]	I_{DIO_MAX}		200			mA
Inductor peak current[*1]	I_{DIO_LP}				1000	mA
Output voltage[*1]	V_{DIO}	VDD=2.5~4.4V, Io=1~200mA	1.65	1.80	1.95	V
Output feedback voltage	V_{DIO_FB}		1.77	1.80	1.83	V
Maximum operating frequency[*1]	F_{DIO_FMAX}	Io = 0 mA, maximum frequency at start-up			1	MHz
Output start-up time[*1]	T_{DIO}			0.2	0.4	ms
Output ON resistor (H side)	R_{ONH_DIO}				0.3	ohm
Output ON resistor (L side)	R_{ONL_DIO}				0.15	ohm

*1 Design guarantee item when using the recommended parts

DDC_ANA

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Maximum output current*1	I_{DANA_MA}		6			mA
Inductor peak current*1	I_{DANA_LP}				150	mA
Output voltage*1	V_{DANA}	VDD=2.5~4.4V, Io=0~6mA, VO_D_ANA[5:0] = 0Ch	0.65	0.70	0.75	V
Output feedback voltage	V_{DANA_FB}	VO_D_ANA[5:0] = 0Ch	0.690	0.700	0.710	V
Maximum operating frequency*1	F_{DANA_FMAX}	Io=0mA, maximum frequency at start-up			2	MHz
Output start-up time*1	T_{DANA}			0.5	1	ms
Output ON resistor (H side)	R_{ONH_DANA}				2	ohm
Output ON resistor (L side)	R_{ONL_DANA}				1	ohm

*1 Design guarantee item when using the recommended parts

DDC_CORE

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Maximum output current*1	I_{DCORE_MA}		100			mA
Inductor peak current*1	I_{DCORE_LP}				500	mA
Output voltage 1*1	V_{DCORE1}	VDD=2.5~4.4V, Io=0~100mA, VO_D_CORE[5:0] = 0Ch	0.65	0.70	0.75	V
Output voltage 2*1	V_{DCORE2}	VDD=2.5~4.4V, Io=0~100mA, VO_D_ CORE [5:0] = 24h	0.90	1.00	1.10	V
Output feedback voltage	V_{DCORE_FB}	VO_D_ CORE [5:0] = 0Ch	0.69	0.70	0.71	V
Maximum operating frequency*1	F_{DCORE_FMAX}	Io = 0 mA, maximum frequency at start-up			2	MHz
Output start-up time*1	T_{DCORE}			0.4	1	ms
Output ON resistor (H side)	R_{ONH_DCORE}				0.8	ohm
Output ON resistor (L side)	R_{ONL_DCORE}				0.6	ohm

*1 Design guarantee item when using the recommended parts

LDO_EMMC

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PSRR LDO_IN	$PSRR_{LEMMC}$	1kHz~100KHzPeak（Io=0A, 100mA）		30		dB
Maximum output current	$I_{LEMMCmax}$		100			mA
Output voltage	V_{LEMMC}	Register setting: VO_L_EMMC[1:0] = 00h (Default)	3.15	3.3	3.45	V
Input stability	$V_{LEMMCivs}$	VDD= V_{LEMMC} +0.2~4.4V			10	mV
Output stability	$V_{LEMMCAls}$	Io=0~100mA			2	mV
Voltage difference between input and output	$V_{LEMMCIO}$	LDO_EMMC_IN = 3.0 V, Io = 100 mA, Vo = 3.3 V settings	2.8			V

LDO_PERI

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PSRR LDO_IN	$PSRR_{LPERI}$	1kHz~100KHzPeak（Io=0A, 10mA）		30		dB
Maximum output current	$I_{LPERImax}$		10			mA
Output voltage	V_{LPERI}	Register setting: VO_L_PERI[1:0] = 00h (Default)	3.15	3.3	3.45	V
Input stability	$V_{LPERIvs}$	VDD=2.5~4.4V			10	mV
Output stability	$V_{LPELIls}$	Io=0~10mA			2	mV
Voltage difference between input and output	$V_{LPELIIO}$	LDO_EMMC_IN=3.0V, Io=10mA, Vo=3.3V settings	2.8			V

LDO_ANA

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Input voltage range	V_{LANA_IN}		V_{LANA} +0.2		VDD	V
PSRR LDO_IN	$PSRR_{LANA1}$	10kHz～2MHzPeak（Io=0A, 100uA, 1mA, 6mA）		55		dB
PSRR VDD	$PSRR_{LANA2}$	10kHz～2MHzPeak（Io=0A, 100uA, 1mA, 6mA）		50		dB
Maximum output current	$I_{LANAmax}$		6			mA
Output voltage	V_{LANA}	Register setting: VO_L_ANA[5:0] = 0Ch (Default)	0.65	0.700	0.75	V
Input stability	$V_{LANAivs}$	VDD=2.5~4.4V			3	mV
Output stability	V_{LANAls}	Io=0~6mA			2	mV

1.0V output for USBPHY (LDO_USB10)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PSRR LDO_IN	$PSRR_{LVIN2}$	1kHz~100KHzPeak（Io=0A, 10mA）		30		dB
Maximum output current	$I_{USB10max}$	* Max. 50 mA due to overcurrent limiter	10		50	mA
Output voltage	V_{USB10}		0.95	1.00	1.05	V
Input stability	$V_{LUSB10ivs}$	VIN=2.5~5.5V			10	mV
Output stability	$V_{LUSB10ls}$	Io=0~10mA			2	mV

List of DC-DC converter and LDO output register settings

Setting voltage of each power supply and code Unit[V]

Address	DDC_ANA	DDC_CORE	LDO_ANA	LDO_EMMC	LDO_PERI
00h		0.55		3.3	3.3
01h		0.5625		3.2	3.2
02h		0.575		3.1	3.1
03h		0.5875		3.0	3.0
04h	0.6	0.6	0.6	2.9	2.9
05h	0.6125	0.6125	0.6	2.8	2.8
06h	0.625	0.625	0.625	2.7	2.7
07h	0.6375	0.6375	0.625	2.6	2.6
08h	0.65	0.65	0.65	2.5	2.5
09h	0.6625	0.6625	0.65	2.4	2.4
0Ah	0.675	0.675	0.675	2.3	2.3
0Bh	0.6875	0.6875	0.675	2.2	2.2
0Ch	0.7	0.7	0.7	2.1	2.1
0Dh	0.7125	0.7125	0.7	2.0	2.0
0Eh	0.725	0.725	0.725	1.9	1.9
0Fh	0.7375	0.7375	0.725	1.8	1.8
10h	0.75	0.75	0.75		
11h	0.7625	0.7625	0.75		
12h	0.775	0.775	0.775		
13h	0.7875	0.7875	0.775		
14h	0.8	0.8	0.8		
15h	0.8125	0.8125	0.8		
16h	0.825	0.825	0.825		
17h	0.8375	0.8375	0.825		
18h	0.85	0.85	0.85		
19h	0.8625	0.8625	0.85		
1Ah	0.875	0.875	0.875		
1Bh	0.8875	0.8875	0.875		
1Ch	0.9	0.9	0.9		
1Dh	0.9125	0.9125	0.9		
1Eh	0.925	0.925	0.925		
1Fh	0.9375	0.9375	0.925		
20h	0.95	0.95	0.95		
21h	0.9625	0.9625	0.95		
22h	0.975	0.975	0.975		
23h	0.9875	0.9875	0.975		
24h	1.0	1.0	1.0		

Unit[V]

Address	DDC_ANA	DDC_CORE
25h	1.0125	1.0125
26h	1.025	1.025
27h	1.0375	1.0375
28h	1.05	1.05
29h	1.0625	1.0625
2Ah	1.075	1.075
2Bh	1.0875	1.0875
2Ch	1.1	1.1
2Dh	1.1125	1.1125
2Eh	1.125	
2Fh	1.1375	
30h	1.15	
31h	1.1625	
32h	1.175	
33h	1.1875	
34h	1.2	
35h	1.2125	
36h	1.225	
37h	1.2375	
38h	1.25	
39h	1.2625	
3Ah	1.275	

* Blue cell values cannot be set (input).
* Yellow cell values are the default settings

◆Analog front-end block for battery power level detection

(Unless otherwise specified: Ta = 27 °C, VBAT = VSYS = VDD_AFE = 3.6 V)

Power supply input (AFE_VDD)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Supply voltage range	V_{DD}		2.5		4.4	V
Operating power consumption	I_{AVD_ACT}	At the time of measurement		100	200	μA
Current consumption when stopped	I_{AVD_SLP}				0.2	μA

Battery voltage, battery temperature measurement (VBAT_VS, TH)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Battery voltage measurement range		VBAT_VS voltage measurement	2.5		4.5	V
Battery voltage measurement resolution				1.1		mV/LSB
Battery voltage measurement accuracy			-4.4(-4)		+4.4(4)	mV(LSB)
Measurement cycle*2		Register：82h/83h ※Default 125ms	125ms		18.2h	
Battery temperature measurement range		TH voltage measurement	0		2.0	V
Battery temperature measurement resolution				0.5		mV/LSB
Battery temperature measurement accuracy			-1		+1	℃
Measurement cycle*2		Register：82h/83h ※Default 125ms	125ms		18.2h	

*2 Measurement is performed at a 7.8 ms cycle during charge.

Battery charge / discharge current measurement (VBT_CS, VSYS_CS)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Current measurement range		Between VSYS_CS and VBAT_CS	-50		50	mV
Current measurement resolution		Between VSYS_CS and VBAT_CS		30		uV/LSB
Current measurement accuracy		Between VSYS_CS and VBAT_CS =10mV	-5		+5	%
Current measurement offset		When VSYS_CS=VBAT_CS (0mA setting) output	-5	0	+5	LSB
Measurement cycle *2		Register：82h/83h ※Default 125ms	125ms		18.2h	

*2 Measurement is performed at a 7.8 ms cycle during charge.

Battery temperature detection and control (VREF, TH_REF)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Reference voltage	V_{ref}			2		V
Reference voltage SW_ON resistor	R_{ON_THREF}	I_{THSW} = 20uA	-	(10)	100	Ω

* Shared with the charge control block

◆Charge control block

(Unless otherwise specified: Ta = 27 °C, VIN = 5V, VBAT=3.6V)

Power path control, shared (VIN, VBT, VSYS)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
VIN detection L side	V_{vinl}	When the VIN voltage rises * 200 mV hysteresis	3.6	3.8	4.0	V
VIN detection H side	V_{vinh}	When the VIN voltage rises * 100 mV hysteresis	5.6	5.8	6.0	V
VSYS detection relative to VIN	V_{inbat}		VSYS -0.2	VSYS -0.1	VSYS	V
Battery discharge current 1	I_{dc1}	VIN=5V, VBAT=4.2V, when power supply block stopped, charge complete			2	uA
Battery discharge current 2	I_{dc2}	VIN=0V , VBAT=4.2V , when power supply block stopped			1	uA
Circuit current	I_{cc}	VIN=5V , when power supply block stopped ※VIN current			1	mA
Chip temperature control	T_{cc}	* Design guarantee item		100		℃
Thermal shutdown	T_{sd}	* Design guarantee item		150		℃

* The battery discharge current is measured at the VSYS pin.

Battery voltage detection and control (VBAT)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Precharge start voltage	$V_{pcstart}$	When the VBAT voltage rises	1.3	1.4	1.5	V
Weak battery judgment voltage	$V_{weakbat}$	When the VBAT voltage rises	3.3	3.4	3.5	V
		Resistor variable range 20mV-step	2.6	-	3.6	V
Rapid charge start voltage	$V_{qcstart}$	When the VBAT voltage rises	2.9	3.0	3.1	V
		Resistor variable range 200mV-step	2.6	-	3.2	V
Charge control voltage	V_{chg}	Ichg=10mA ※Ta=0~60℃	4.17	4.20	4.23	V
		Resistor variable range 50mV-step	4.0	-	4.4	V
Recharge start voltage	$V_{rcstart}$	During VBAT voltage step down	V_{chg}-0.45	V_{chg}-0.4	V_{chg}-0.35	V
		Resistor variable range 100mV-step	V_{chg}-0.4	-	V_{chg}-0.25	V
Charge complete voltage	V_{fv}	Function enable/disable is selected by the register. * Default: enable		$V_{rcstart}$+0.1		V

Charge current detection and control (CHG_ISET)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Rapid charge current	I_{chg}	Riset=33kohm , VBAT=3.6V	250	300	350	mA
Precharge current	I_{pchg}	Riset=33kohm , VBAT=2.2V, ※I_{chg}*0.2		60		mA
Initial charge current	I_{ppchg}	VBAT=1.0V	5	10	20	mA
Charge complete current	I_{fc}	When setting to 30mA	25	30	35	mA
		Resistor variable range10mA-step	10	-	50	mA

* The charge current can be varied by an external resistor. :Ichg=10000/Riset

Battery temperature detection and control (VREF, TH)

※The thermistor resistor for temperature measurement assumes the NCP15WF104F03RC

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Reference voltage for temperature detection	T_{ref}	Ro=200kohm		2		V
Battery connection detection	T_{thc}			T_{ref}*0.9		V
Temperature detection 1-1*3	T_{th1-1}	Hysteresis of 2.5°C on the temperature rise side relative to 0°C		0		℃
Temperature detection 1-2*4	T_{th1-1}		0.0		15.0	℃
Temperature detection 2*3	T_{th2}	Hysteresis of 2.5°C on the temperature rise side relative to 10°C		10		℃
Temperature detection 3*3	T_{th3}	Hysteresis of 2.5°C on the temperature rise side relative to 45°C		45		℃
Temperature detection 4-1*3	T_{th4-1}	Hysteresis of 2.5°C on the temperature rise side relative to 60°C		60		℃
Temperature detection 4-2*4	T_{th4-2}		45.0		60.0	℃

*3 Judged by the digital comparator output (set by 78h to 7Fh)

*4 Temperature detection 1-2 and 4-2 are when VBAT < $V_{qcstart}$ (before rapid charge, before HOST start-up).

3.3V output for USBPHY (LDO_USB33)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
PSRR LDO_IN	$PSRR_{LVIN1}$	1kHz~100KHzPeak（Io=0A, 10mA）		-20		dB
Maximum output current	$I_{USB33max}$	* Max. 50 mA due to overcurrent limiter	10		50	mA
Output voltage	V_{USB33}		3.2	3.3	3.4	V
Input stability	$V_{LUSB33ivs}$	VIN=4.5~5.5V			10	mV
Output stability	$V_{LUSB33ls}$	Io=0~10mA			2	mV

USB detection (DP, DM, DLINE_SW)

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
DP pin output voltage	V_{dp}	I_{dpo}=0~150uA	0.5	0.6	0.7	V
DP pin maximum source current	I_{dp}		150			uA
DM pin sink current	I_{dm}	V_{dpo}=0.6V	50		150	uA
Voltage detection	V_{dpm}		0.25		0.4	V
DLINE_SW pin H level output voltage	V_{ODL_H}	I_{OUT} =-2mA	V_{USB33} − 0.2V	-	-	V
DLINE_SW pin L level output voltage	V_{ODL_L}	I_{IN} =+2mA	-	-	0.2	V

Timers and setup times

Item	Symbol	Measurement conditions	Min	Typ.	Max	Unit
Initial charge timer	T_{ppc}		7	10	13	sec
Weak Battery timer	T_{wb}		24	34	44	min
Precharge timer	T_{pc}	Changeable to 120 min by the register	54	60	66	min
Rapid charge timer	T_{qc}	Changeable to 300 min by the register	540	600	660	min
Battery voltage setup time Battery temperature setup time	T_{bvd}	Setup by the 31 ms-clk matching 4 times Setup by the 31 ms-clk matching 4 times	3		4	Clk
Charge current setup time	T_{bcd}	Setup by the 250ms-clk matching 4 times * Changeable to x10 by the register	3		4	Clk

◆Audio block

MICs to serial output characteristics

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC = 1.8 V, DVDD = 1.8 V, VBAT = 3.7 V, GND_MIC =DGND = 0 V, OSCIN = 512•48 kHz, Input test signal is a 1 kHz sine wave, Measurement bandwidth is 20 Hz to 20 kHz)

Parameters	Symbol	Min	Typ	Max	Condition	Units
Input impedance	RMICIN		50			kΩ
DC voltage at MICx	VCM	-	AVDD_MIC/2	-		V
Full-scale input voltage	FSMIC	-	AVDD_MIC/2	-		Vpp
Signal to noise ratio	SNRMIC	-	90	-	A-weight, MICGAINx=0dB	dB
THD+N	THDMIC	-	-80	-	-6dBFS, MICGAINx=0dB	dB
Dynamic range	DRMIC	-	90	-	A-weight, MICGAINx=0dB	dB
Crosstalk	CTMIC	-	100	-	1kHz	dB
MICGAIN range	MICGAINx	0	-	15		dB
MICGAIN step	MICSTEPx	2.9	3	3.1		dB
PGAGAIN range	PGAGAINx	0	-	6		dB
PGAGAIN step	PGASTEPx	0.4	0.5	0.6		dB

Serial input to SPOUTs characteristics (Loop OFF)

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC = 1.8 V, DVDD = 1.8 V, VBAT = 3.7 V, AGND_MIC = DGND = 0 V, OSCIN = 512•48 kHz, Input test signal is a 1 kHz sine wave, Measurement bandwidth is 20 Hz to 20 kHz, test load R_L = 8Ω, C_L = 150 pF for bridge tied an ear speaker load.)

Parameters	Symbol	Min	Typ	Max	Condition	Units
Power output per channel	PO	-	400	-	0dB FS input/Codec gain=24dB	mW
Total harmonic distortion + noise	THDSP	-	-60	-54	Input Amplitude=-6dBFS	dB
Output Noise	Vnoise	-	10	-	A-weight	uVrms

Serial input to SPOUTs characteristics (Loop ON)

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC = 1.8 V, DVDD = 1.8 V, VBAT = 3.7 V, AGND_MIC = DGND = 0 V, OSCIN = 512•48 kHz, Input test signal is a 1 kHz sine wave, Measurement bandwidth is 20 Hz to 20 kHz, test load R_L = 8Ω, C_L = 150 pF for bridge tied an ear speaker load.)

Parameters	Symbol	Min	Typ	Max	Condition	Units
Power output per channel	PO	-	400	-	0dB FS input/Codec gain=24dB	mW
Total harmonic distortion + noise	THDSP	-	-66	-60	Input Amplitude=-6dBFS	dB
Output Noise	Vnoise	-	10	-	A-weight	uVrms

DC characteristics

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC = 1.8 V, DVDD = 1.8 V, VBAT = 3.7 V, AGND_MIC = DGND = 0 V, OSCIN = 512•48 kHz)

Parameters	Symbol	Min	Typ	Max	Condition	Units
MICx_BIAS						
	VO_{MICBS}	-	0	-	Low Output mode	V
		1.8	2.0	2.2		
		-	Hi-Z	-	Stand by mode	
Output current	IO_{MICBS}	-	-	2.0	low noise mode	mA
Output noise	NO_{MICBS}	-	-	5	low noise mode	μVrms
Output impedance	RO_{MICBS}	40	60	80	low noise mode	Ω
Output impedance	RO_{MICBS}	-	60	-	low power mode	
		16k	20k	24k		
		80k	100k	120k		
LDO for MICIN						
LDOOUT voltage	VREG18	1.62	1.8	1.98		V

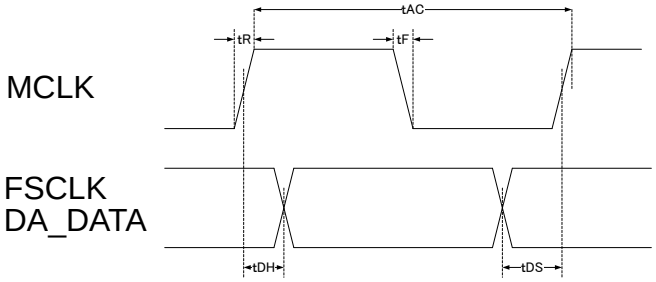
Crystal switching specification

(Unless otherwise specified: Ta = 25 °C, AVDD_MIC =.8 V, DVDD = 1.8 V, VBAT = 3.7 V, AGND_MIC = DGND = 0 V)

Parameters	Symbol	Min	Typ	Max	Condition	Units
XI_A frequency	FREQ	-	24.576	-		MHz
		-	49.152	-		

Switching specifications and characteristics (serial audio interface form CXD5602)

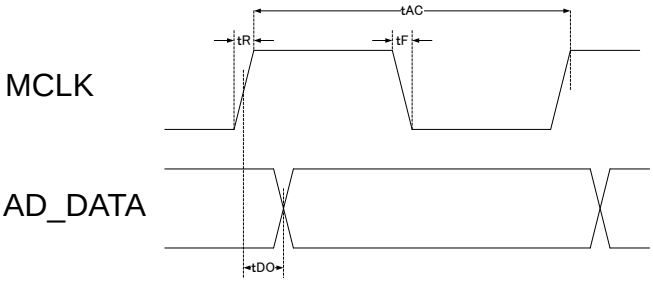
Parameters	Symbol	Min	Typ	Max	Condition	Units
Serial data input1 - FSCLK/DA_DATA						
MCLK clock frequency	-	-	24.576	-		MHz
MCLK clock duty cycle	-	40	50	60		%
MCLK clock period	tAC		40.69			ns
Rise time	tR			5.0		ns
Fall time	tF			5.0		ns
Setup time	tDS	5.0				ns
Hold time	tDH	0.0				ns



MCLK/FSCLK/DA_DATA timing

Switching specifications and characteristics (serial audio interface to CXD5602)

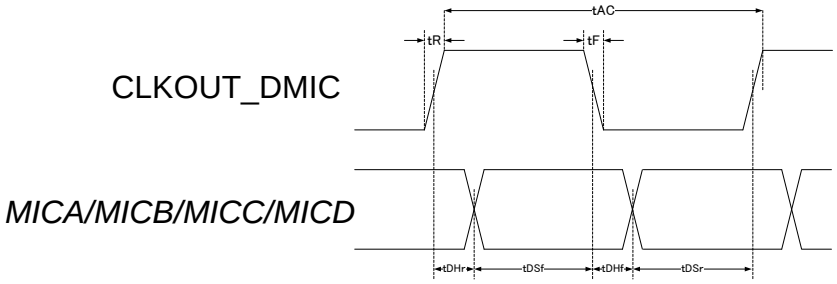
Parameters	Symbol	Min	Typ	Max	Condition	Units
Serial data output - MCLK/AD_DATA						
MCLK clock frequency	-	-	24.576	-		MHz
MCLK clock duty cycle	-	40	50	60		%
MCLK clock period	tAC		40.69			ns
Rise time	tR			5.0		ns
Fall time	tF			5.0		ns
Data Delay	tDO	3.0		15.0		ns



MCLK/AD_DATA timing

Digital microphone interface

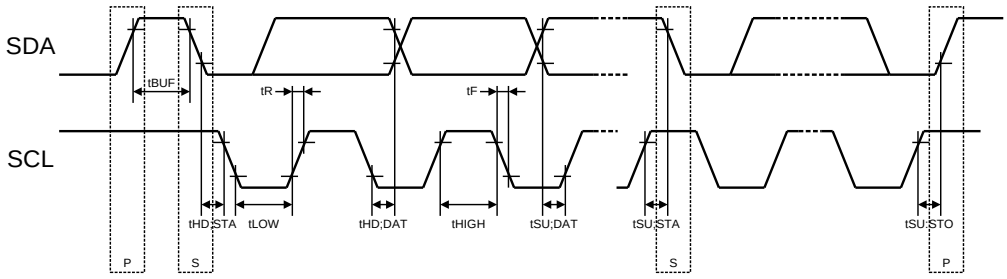
Parameters	Symbol	Min	Typ	Max	Condition	Units
Digital MIC input1 - DMCLK = 3.072 MHz						
CLKOUT_DMIC clock frequency	-	-	3.072	-		MHz
CLKOUT_DMIC clock duty cycle	-	40	50	60		%
CLKOUT_DMIC clock period	tAC		325.52			ns
Rise time	tR			5.0		ns
Fall time	tF			5.0		ns
Setup time	tDSr/tDSf	5.0				ns
Hold time	tDHf/tDHr	0.0				ns
Digital MIC input1 - DMCLK = 1.024 MHz (DDR input)						
CLKOUT_DMIC clock frequency	-	-	1.024	-		MHz
CLKOUT_DMIC clock duty cycle	-	40	50	60		%
CLKOUT_DMIC clock period	tAC		976.56			ns
Rise time	tR			5.0		ns
Fall time	tF			5.0		ns
Setup time	tDSr/tDSf	5.0				ns
Hold time	tDHf/tDHr	0.0				ns



DMCLK/DMIC timing

I2C bus switching specification

Parameters	Symbol	Min	Typ	Max	Condition	Units
Clock frequency	f_{SCL}	0	-	400		kHz
Data charge minimum waiting time	t_{BUF}	1.3	-	-		µs
Data transfer start waiting time	$t_{HD:STA}$	0.6	-	-		µs
Low level clock pulse width	t_{LOW}	1.3	-	-		µs
High level clock pulse width	t_{HIGH}	0.6	-	-		µs
Start setup waiting time	$t_{SU:STA}$	0.6	-	-		µs
Data hold time	$t_{HD:DATA}$	0	-	-		µs
Data setup time	$t_{SU:STA}$	100	-	-		ns
Rise time	t_R	-	-	300		ns
Fall time	t_F	-	-	300		ns
Stop setup waiting time	$t_{SU:STO}$	0.6	-	-		µs



I2C timing

digital input / output signal threshold level

Parameters	Symbol	Min	Typ	Max	Condition	Units
High-level output voltage	V_{OH}	DVDD - 0.2	-	-		V
Low-level output voltage	V_{OL}	-	-	0.2		V
High-level input voltage	V_{IH}	0.7 x DVDD	-	-		V
Low-level input voltage	V_{IL}	-	-	0.3 x DVDD		V

Power consumption (audio block)

The table below lists the current consumed by each Adonis internal power supply pin. This enables to calculate the overall power in accordance with the use case.

Block	Operating state	Pin	Min	Typ	Max	Condition	Unit
Logic	When reset	DVDD		0.1	-		uA
	Analog Mic input SPOUT output				5	When Xtal 24.576MHz FSCLK/AD_DATA pin load 10 pF	mA
MICIN	Sleep	AVDD_MIC			10		uA
	1ch operation				3.6	Typ: approximately 2.5 mA	mA
	2ch operation				6.6	Typ: approximately 5 mA	mA
	4ch operation				12.6	Typ: approximately 10 mA	mA
	Digital MIC				1	When using Digital MIC	mA
Crystal buffer	Sleep	VBAT2		0.05	2	XRESET=Low	uA
	24.576MHz			1	1.5	SPOUT not used, oscillation stable	mA
	49.152MHz			1.2	1.8	SPOUT not used, oscillation stable	mA
	24.576MHz mono			1.1	1.65	SPOUT BTL mono, oscillation stable	mA
	24.576MHz Stereo			1.2	1.8	SPOUT BTL stereo, oscillation stable	mA
	49.152MHz mono			1.4	2.1	SPOUT BTL mono, oscillation stable	mA
	49.152MHz Stereo			1.6	2.4	SPOUT BTL stereo, oscillation stable	mA
MICBIAS	Sleep	VBAT1		0.05	1		uA
	MICBIAS 1ch			0.23	0.32	MICBIAS only operating	mA
	MICBIAS 2ch			0.16	0.24		mA
MICINLDO	Active			1.2	1.7	MICIN block current not included	mA
SPOUT	Sleep	AVDD_DRV*			0.1		uA
	Stereo 16fs			1.6		BTLstereo24.576MHz Max = about 3.6mA	mA
	Stereo 32fs			3.2		BTL stereo 49.152MHz Max= about 5.34mA	mA
	Stereo 16fs Loop			8.6		BTLstereo24.576MHz, Loop ON Max= about 10.18mA	mA
	Stereo 32fs Loop			7.8		BTL stereo 49.152MHz, Loop ON Max= about 11.94mA	mA

Description of Functions

◆Power supply block

RTC

- Low power consumption IQ = 3 μA(typ.)
- Clock, start-up timer

Voltage step down type PFM control DC-DC converter

- Low power consumption IQ = 10μA (per channel)
- DDC_IO / Vout = 1.8 V/ Iomax = 200mA(min)
- DDC_ANA / Vout = 0.600 V～1.275 V, 25 mV-step / Iomax = 6 mA(min)
- DDC_CORE / Vout = 0.5500 V～1.1125 V, 12.5mV-step / Iomax = 100 mA(min)

LDO

- Low power consumption IQ = 6 μA (1ch per channel)
- LDO_ANA / Vout = 0.600 V～1.000 V, 25 mV-step / Iomax = 6 mA(min)
- LDO_EMMC / Vout = 1.8V～3.3V,100mV-step / Iomax = 100 mA(min)
- LDO_PERI / Vout = 1.8V～3.3V,100mV-step / Iomax = 10 mA(min)
- LDO_USB10 for USB-PHY / Vout = 1.0V/ Iomax = 10 mA(min)

External interface

- Load switch (4ch for 1.8 V)
- Communication (I2C serial interface, 32.768 kHz clock, reset, interrupt start-up control)
- GPO (8 systems, general-purpose switch drive, enable drive)
- USB detection (USB connection signal, Data line switch control signal)

◆Analog front-end block for battery power level detection

- On-chip 12-bit ADC (1ch: time sharing control) for battery power level detection and battery voltage, current and temperature measurement in the CXD5602 System

◆Charge control block

- Standalone type charge function
- Protective function
- Conformity to USB battery charging 1.2 (conformance as a system)
- USB detection (USB connection signal, Data line switch control signal)
- LDO_USB33 for USB-PHY / Vout =3.3V / Iomax = 10 mA(min)

◆Audio block

CXD5247 Audio is an analog audio I/O IC developed for the CXD5602 System. CXD5602 performs signal transfer using an original format. The two crystal types of 24.576 MHz and 49.152 MHz are supported as the clock source. The input systems include a ΔΣ ADC that supports four analog MIC inputs and an 8-channel digital MIC interface. The analog MIC input and digital MIC input pins are shared and used exclusively. The output system is a BTL output Class-D amplifier (L/R). In addition, two systems of MIC bias circuits and a 1.8 V output LDO for MIC input are mounted.

Definition of fs

This specification defines fs as follows: **fs = 48 kHz**

Power Up constraint

CXD5247 Audio power-on (including reset signal assert) is subject to the restrictions noted in the table below.

(When external AVDD_MIC is supplied)

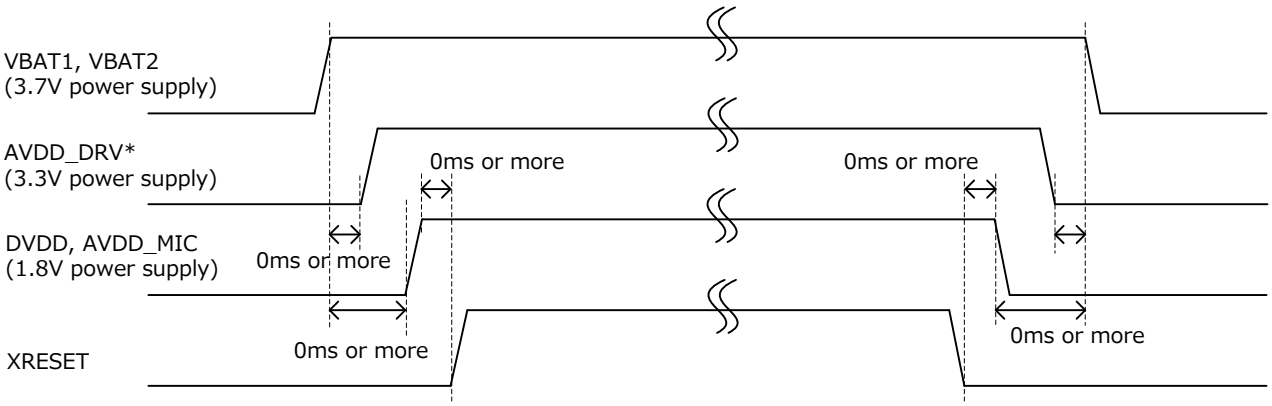
VBAT1/VBAT2	DVDD	AVDD_MIC	AVDD_DRV*	XRESET	Restrictions
OFF	OFF	OFF	OFF	0	**Allowed**
OFF	OFF	OFF	OFF	1	**Not Allowed**
OFF	OFF	OFF	ON	0	**Not Allowed**
OFF	OFF	OFF	ON	1	**Not Allowed**
OFF	OFF	ON	OFF	0	**Not Allowed**
OFF	OFF	ON	OFF	1	**Not Allowed**
OFF	OFF	ON	ON	0	**Not Allowed**
OFF	OFF	ON	ON	1	**Not Allowed**
OFF	ON	OFF	OFF	0	**Not Allowed**
OFF	ON	OFF	OFF	1	**Not Allowed**
OFF	ON	OFF	ON	0	**Not Allowed**
OFF	ON	OFF	ON	1	**Not Allowed**
OFF	ON	ON	OFF	0	**Not Allowed**
OFF	ON	ON	OFF	1	**Not Allowed**
OFF	ON	ON	ON	0	**Not Allowed**
OFF	ON	ON	ON	1	**Not Allowed**
ON	OFF	OFF	OFF	0	**Allowed**
ON	OFF	OFF	OFF	1	**Not Allowed**
ON	OFF	OFF	ON	0	**Allowed**
ON	OFF	OFF	ON	1	**Not Allowed**
ON	OFF	ON	OFF	0	**Allowed**
ON	OFF	ON	OFF	1	**Not Allowed**
ON	OFF	ON	ON	0	**Allowed**
ON	OFF	ON	ON	1	**Not Allowed**
ON	ON	OFF	OFF	0	**Allowed**
ON	ON	OFF	OFF	1	**Allowed**
ON	ON	OFF	ON	0	**Allowed**

ON	ON	OFF	ON	1	**Allowed**
ON	ON	ON	OFF	0	**Allowed**
ON	ON	ON	OFF	1	**Allowed**
ON	ON	ON	ON	0	**Allowed**
ON	ON	ON	ON	1	**Allowed**

Power Up/Reset assert sequence constraint

The CXD5247 Audio power-on sequence and reset cancel restrictions are shown below. Figure shows the timing sequence. (When external AVDD_MIC is applied)

- XRESET is canceled after VBAT1, VBAT2 and DVDD have risen.
- AVDD_DRV* should rise after VBAT1 and VBAT2 have risen.
- AVDD_DRV* also supports use cases when power supply is not turned on.



Power Up sequence

Supported crystals / clocks

This IC supports the following crystal frequencies.

Supported crystal frequencies

Symbol	Frequency	Description
XI_A XO_A	24.576MHz	Master clock, 512fs
	49.152MHz	Master clock, 1024 fs, Hi-Res operation

An external clock (0 V - 1.8 V square wave) can also be applied to the OSCIN pin.

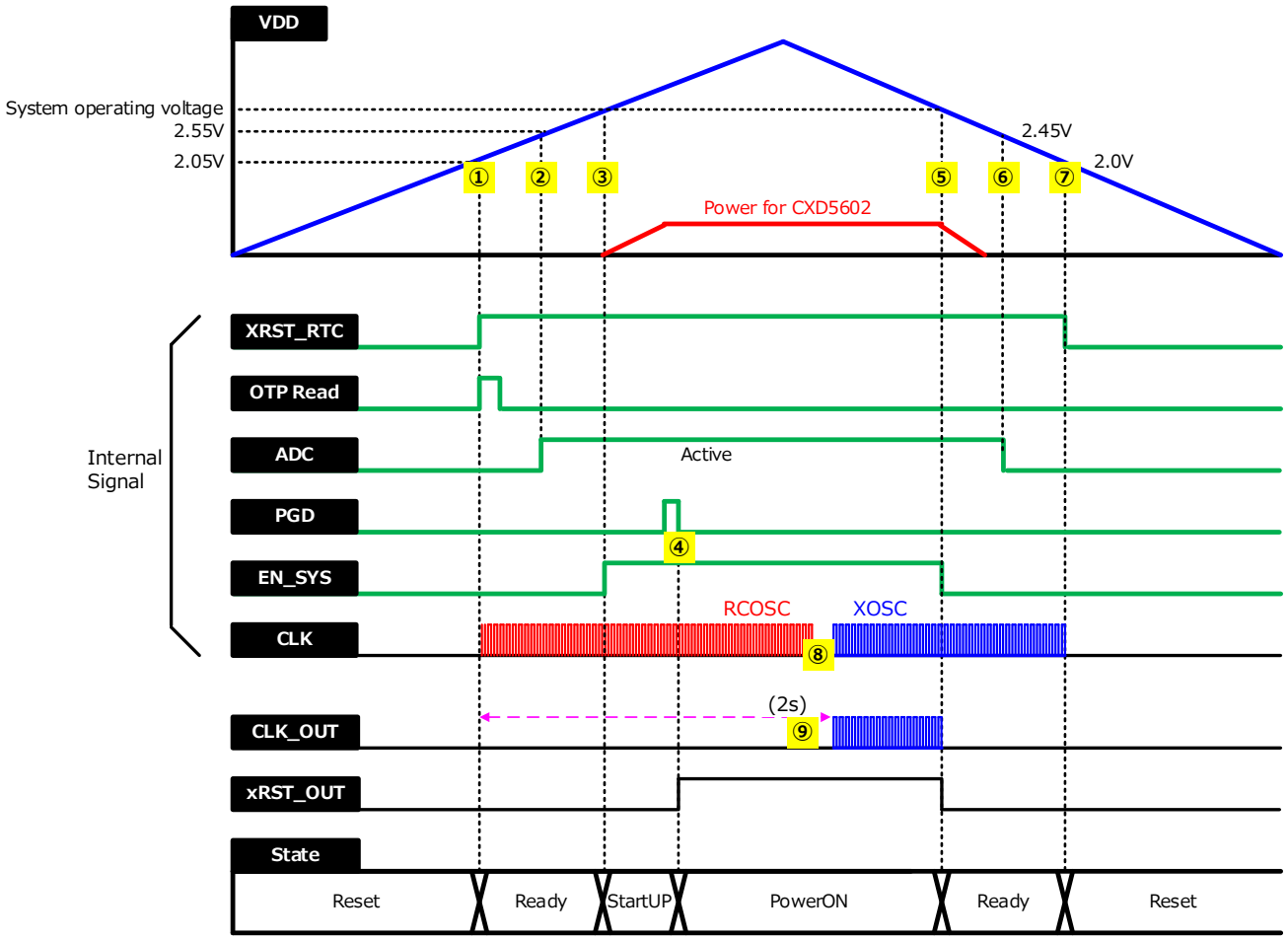
Frequency when applying an external clock

Symbol	Frequency	Description
XI_A	24.576MHz	Master clock, 512fs
	49.152MHz	Master clock, 1024fs Hi-Res operation

Description of Operation

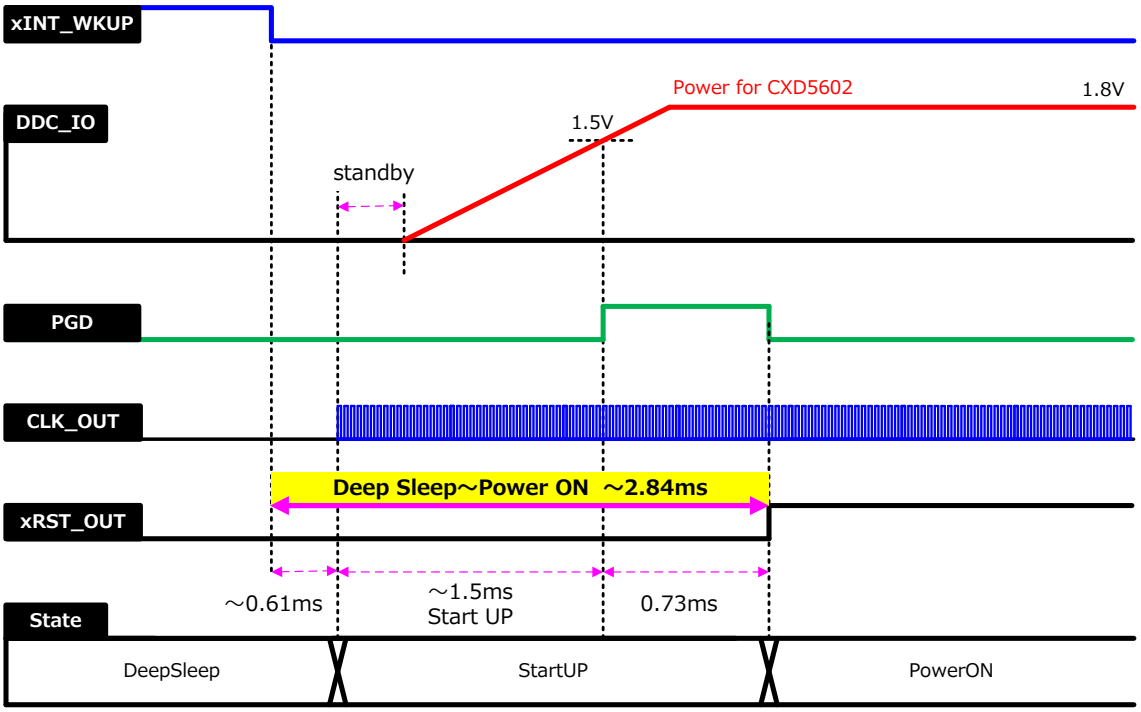
◆Power supply block operation sequence

Timing chart (Start UP to Stop)

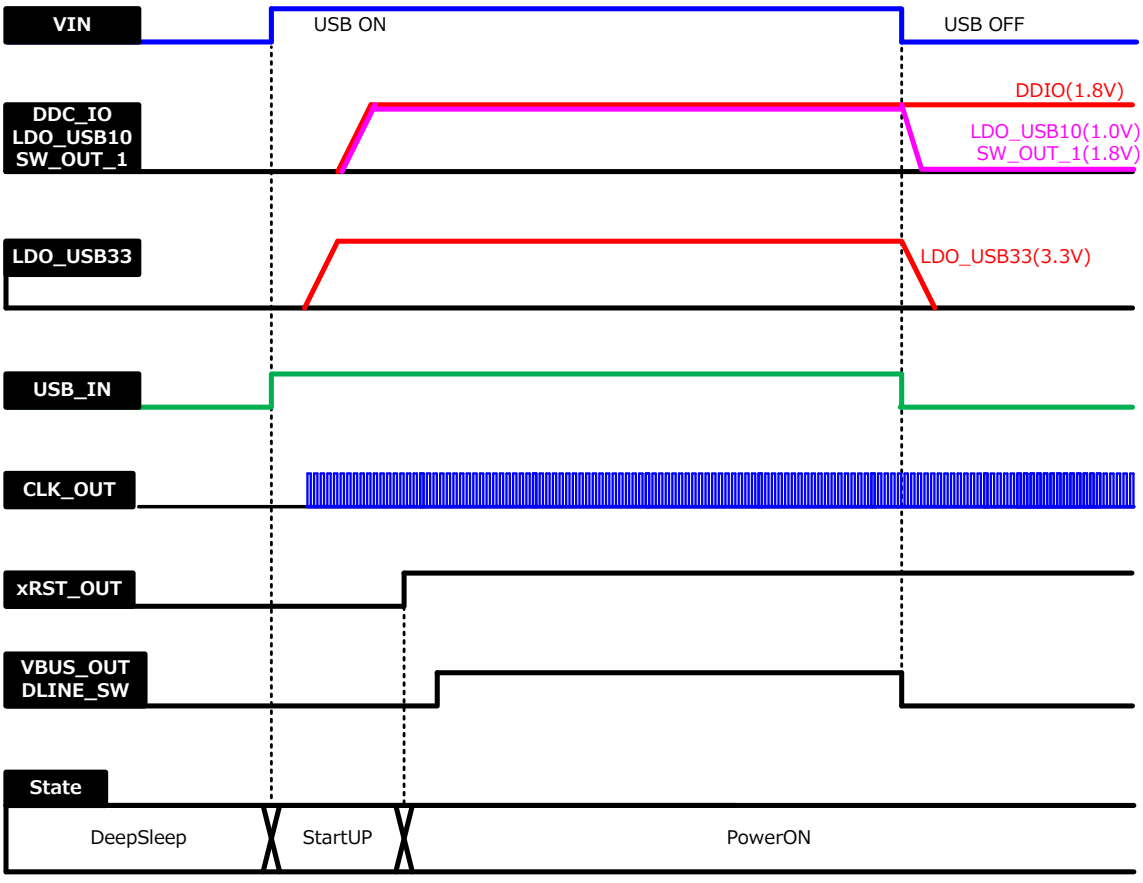


No.	Description	State
1	Detect 2.05 V and cancel the internal circuit reset state. * Read and reflect the OTP data for the analog circuits after reset cancel.	Reset→Ready
2	Detect 2.55 V and start ADC operation. (Only the battery voltage is measured in the Ready state.)	Ready
3	Detect the system operating voltage (3Ch: Def BDh) or more and start up the power supply block. This detection is performed by comparing the register setting value and the ADC data (digital comparator).	Ready→StartUP
4	Perform state transition by detecting the rise of the CXD5602 power supplies (4 systems: DDC_IO/ANA/CORE and LDO_ANA).	StartUP→PowerON
5	Detect the system operating voltage or less and stop power supply output (power supply block operation). * 4-bit (72 mV) hysteresis control is performed on the voltage step down side relative to the 3Ch setting value.	PowerON→Ready
6	Detect 2.45 V (100 mV hysteresis control relative to the rise 2.55 V) and stop ADC operation.	Ready
7	Detect 2.0 V (50 mV hysteresis control relative to the rise 2.05 V) and stop operation.	Ready→Reset
8	Operation uses the internal RC oscillation circuit (15 kHz) until the crystal oscillation circuit (XOSC) starts up. The transition from the RC oscillation circuit to the crystal oscillation circuit is performed automatically inside	–
9	Approximately 2 s (typ.) is required after reset cancel until the crystal oscillation circuit starts up and the clock is output to CXD5602 (output from the CLK_OUT pin).	–

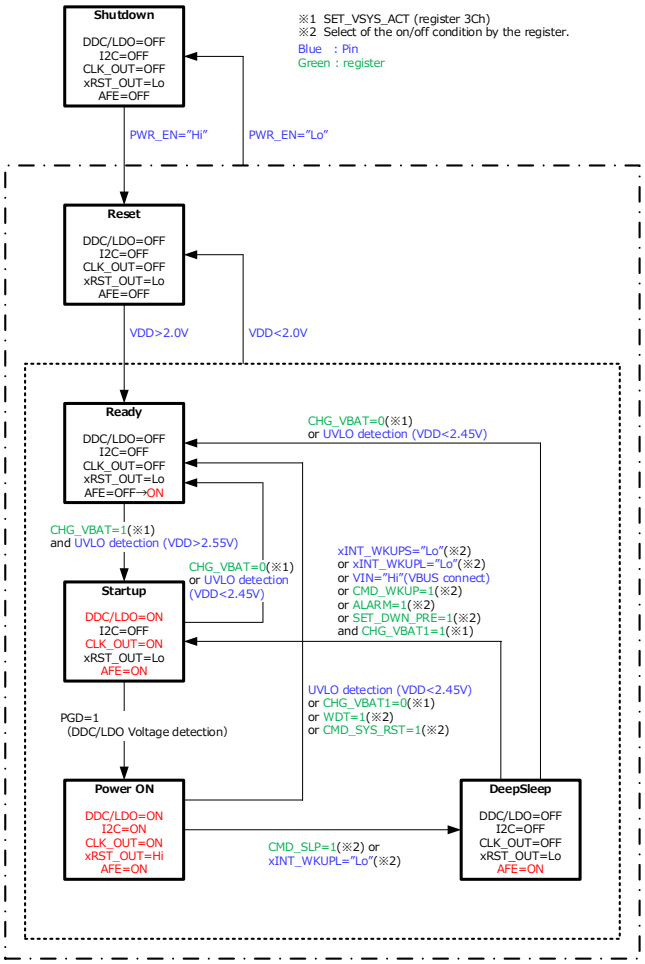
Deep Sleep（xINT_WKUP）～ Power ON



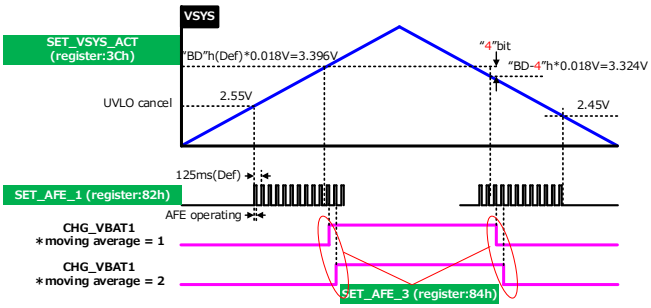
Deep Sleep ～ USB ON～ USB OFF



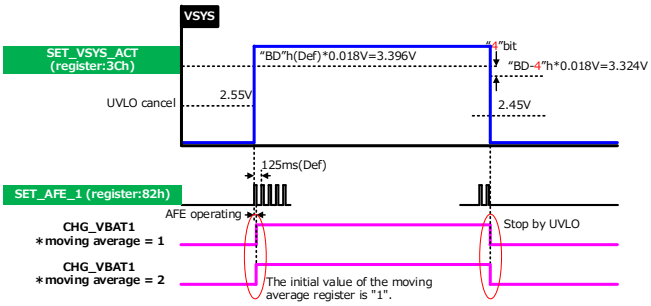
◆Power supply block state transition diagram



Timing chart of CHG_BAT1 (Case the voltage of VSYS rises slowly)

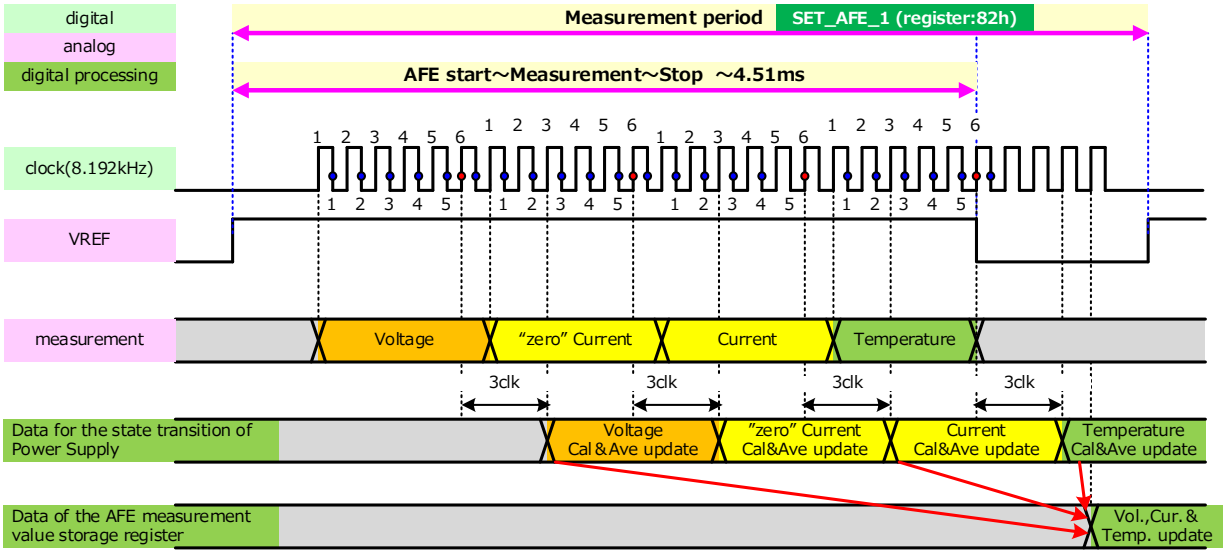


Timing chart of CHG_BAT1 (Case the voltage of VSYS rises quickly)

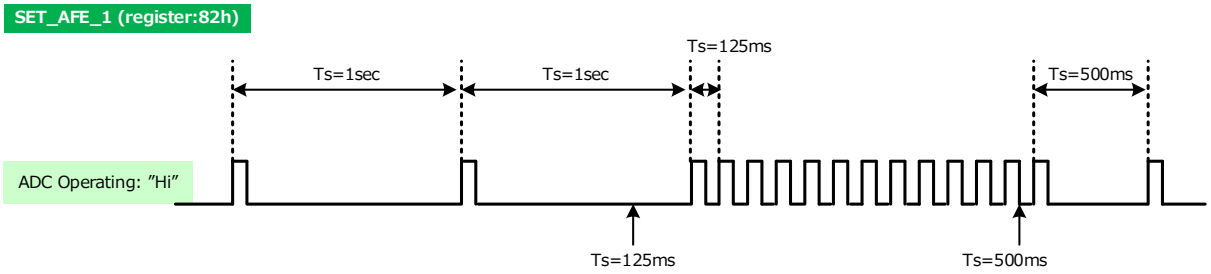


◆AFE block operation timing chart for battery power level detection

Timing chart of AFE operation



Timing chart (During the measurement cycle change)



Battery information measurement value read

The measurement data is reflected to the AFE measurement value storage register (registers 85h to 8Ah and 8Dh to 8Eh) by setting "1" in LRQ_AFE (register 8Bh). LRQ_AFED_STATE (register 8Ch) goes to "1" after the data is reflected.
The moving average values set by SET_AFE3 (register 84h[1:0]) are reflected to the storage registers.

- Battery voltage (DATA_AFEV1,2 register 85h,86h)

Battery voltage = Register value ×1.12mV Ex. : C85h×1.12mV=3.6V

- Battery charge/discharge current (DATA_AFEI1,2 register 87h,88h)

Battery charge/discharge current = (Register value - 800h) ÷ Current detection resistor ×0.02929 Ex. : (6ABh-800h) ÷0.1Ω×0.02929= - 100mA

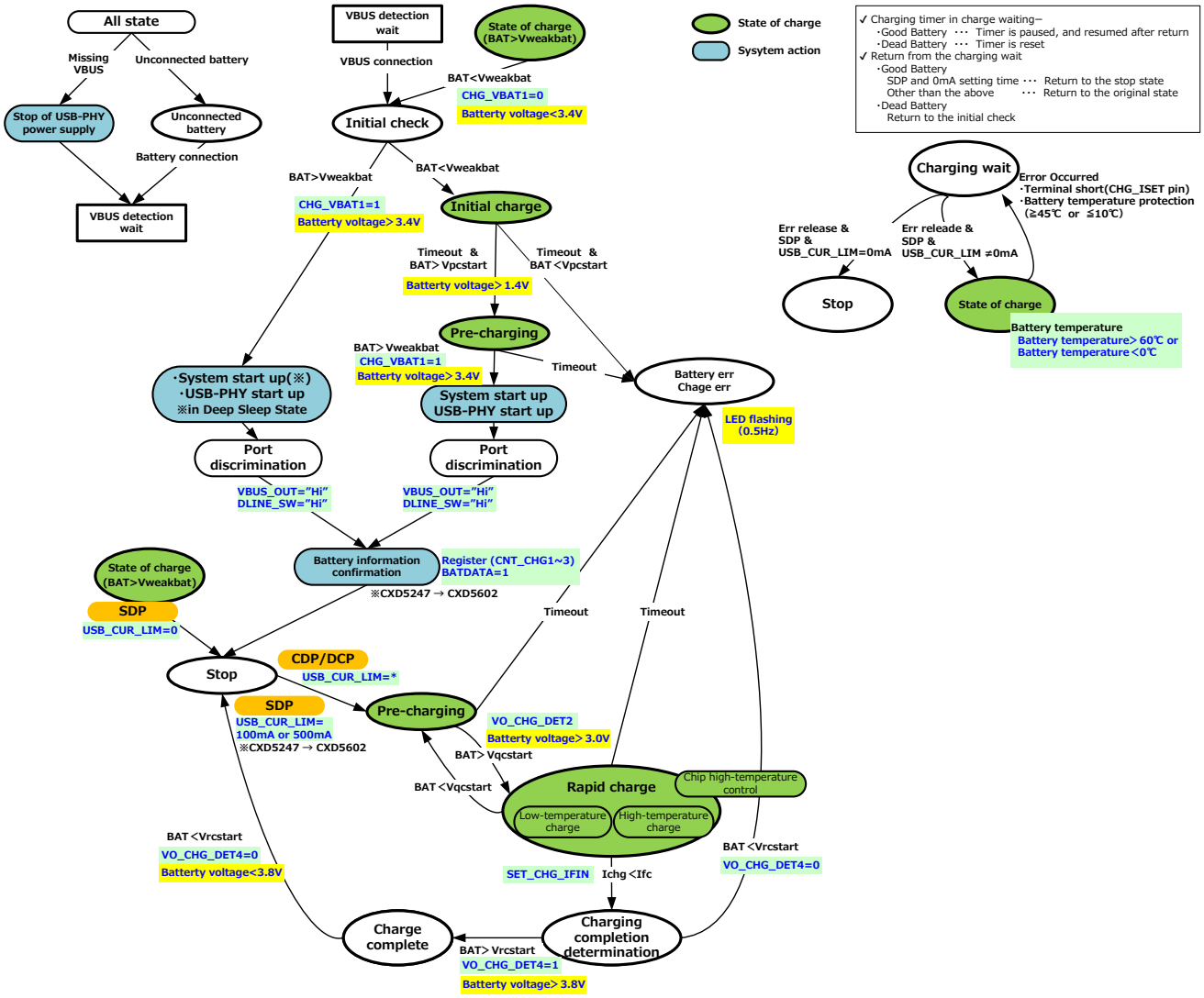
* "−" is the discharge direction and "+" is the charge direction.

- Battery temperature (DATA_AFET1,2 register 89h,8Ah)

Battery temperature (thermistor voltage) = Register value ×0.4883mV Ex.: 712h×0.4883mV=0.884V

* The temperature is determined according to the thermistor resistor (B constant) and the measurement value. When the B constant is B4250K, 0.884 V corresponds to a battery temperature of 30°C.

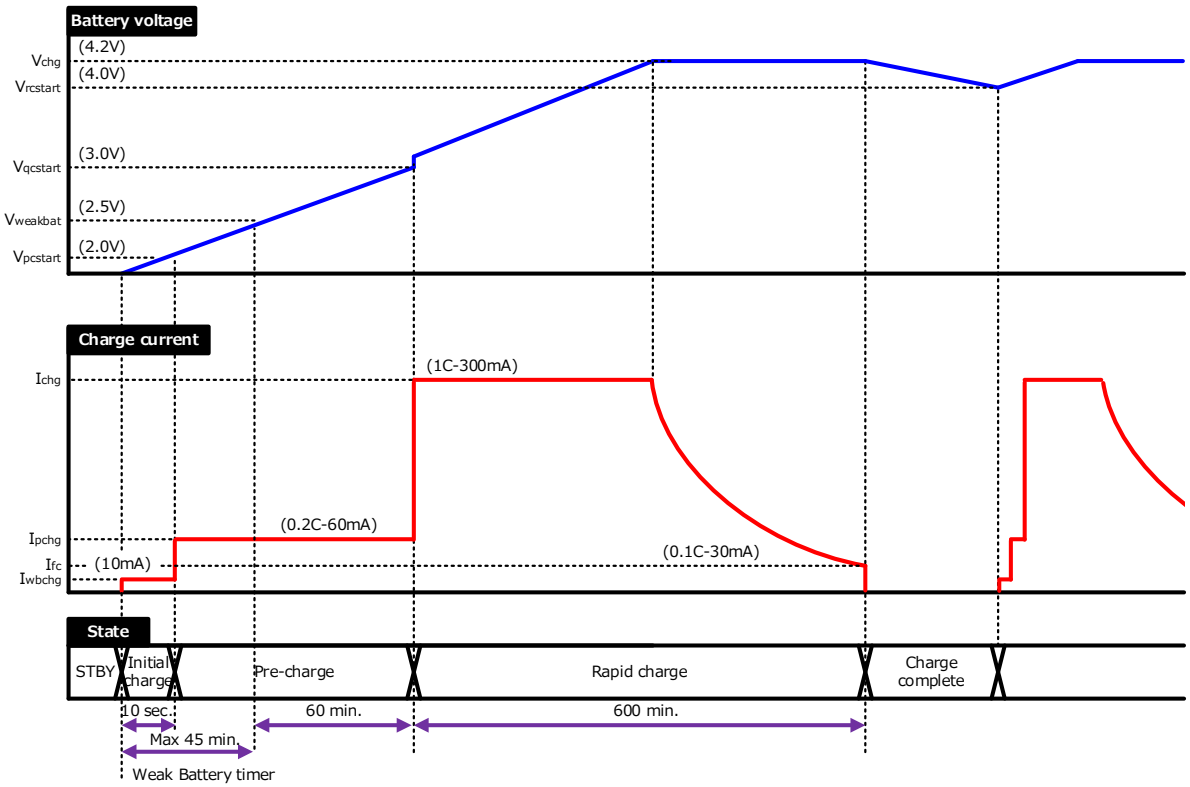
◆Charge control block state transition diagram



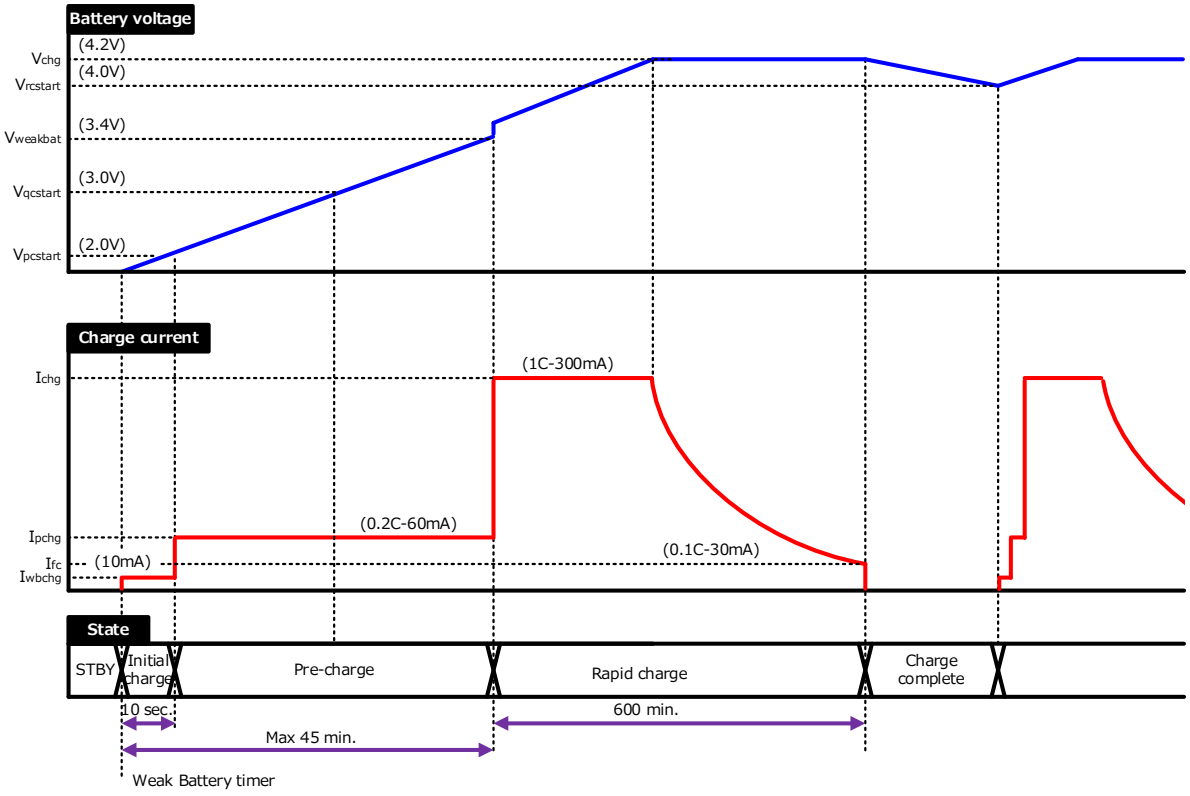
◆Charge control block operation timing

Charge timing chart

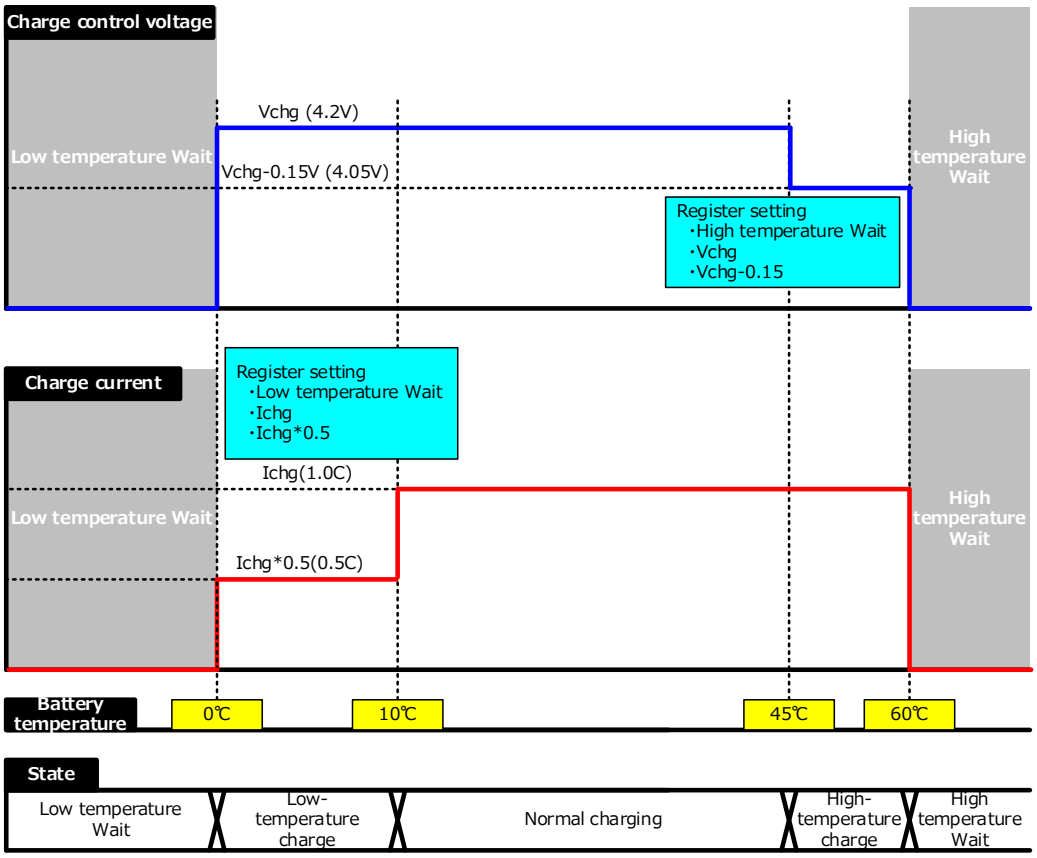
Vqcstart > Vweakbat



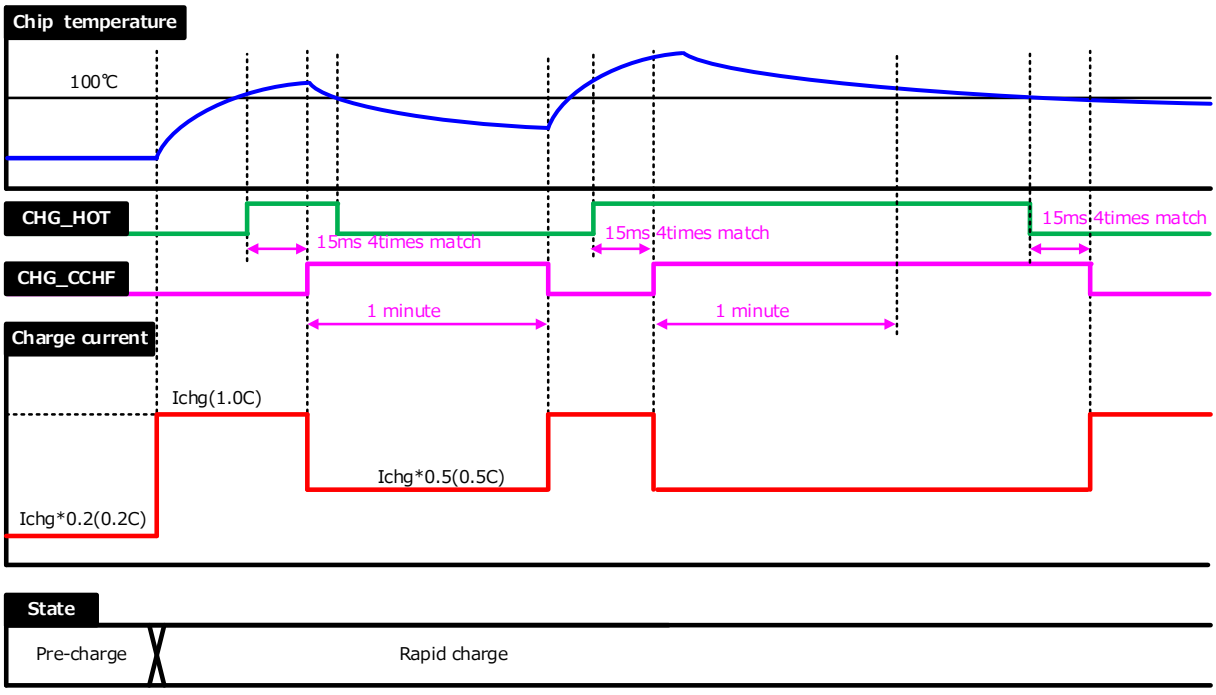
Vqcstart < Vweakbat



JEITA Guidelines

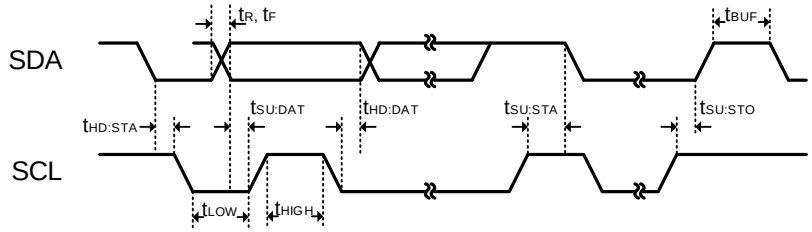


The control by the chip temperature in during Charge



◆Power block – I2C specifications

Symbol	Item	Min.	Max.	Unit
f_{SCL_P}	SCL_P clock frequency	0	400	kHz
$t_{HD:STA}$	Hold time (repeat) start condition (The first clock pulse is generated after this period.)	0.6	-	us
t_{LOW}	SCL_P clock Low period	1.3	-	us
t_{HIGH}	SCL_P clock High period	0.6	-	us
$t_{SU:STA}$	Repeat start condition setup time	0.6	-	us
$t_{HD:DAT}$	Data hold time	0	-	us
$t_{SU:DAT}$	Data setup time	100	-	ns
tr	SDA_P signal and SCL_P signal rise time	-	300	ns
tf	SDA_P signal and SCL_P signal fall time	-	300	ns
$t_{SU:STO}$	Stop condition setup time	0.6	-	us
t_{BUF}	Bus free time between Stop and Start conditions	1.3	-	us
Cb	Capacitance load of each bus line	-	400	pF



Write mode

S	Slave Address	W	A	Sub Address	A	Data	A	P

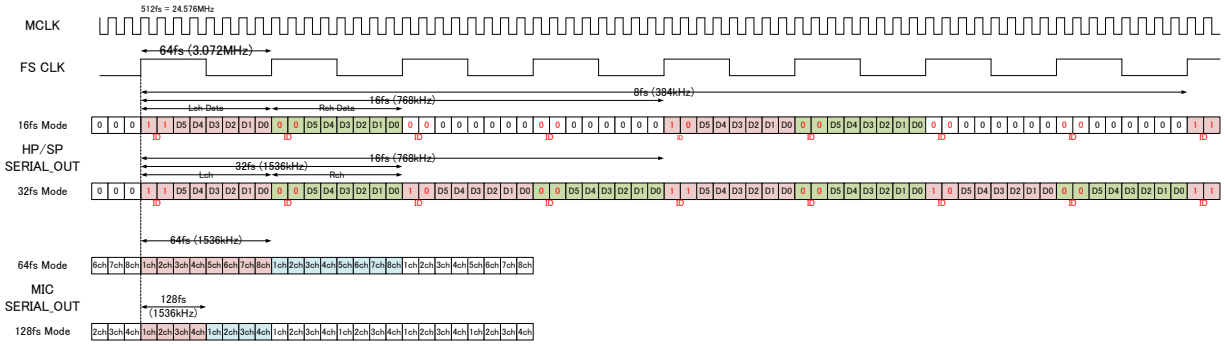
Read mode

S	Slave Address	W	A	Sub Address	A	SR	Slave Address	R	A	Data	N	P

symbol	description	bit
S	Start Condition	-
SR	Repeat Start Condition	-
P	Stop Condition	-
Slave Address	7'h2C	7
W	Write mode (Host→CXD5247)	1
R	Read mode(CXD5247→HOST)	1
A	ACK	1
N	NACK	1
Sub Address	Command Register	8
Data	Write/Read Data	8

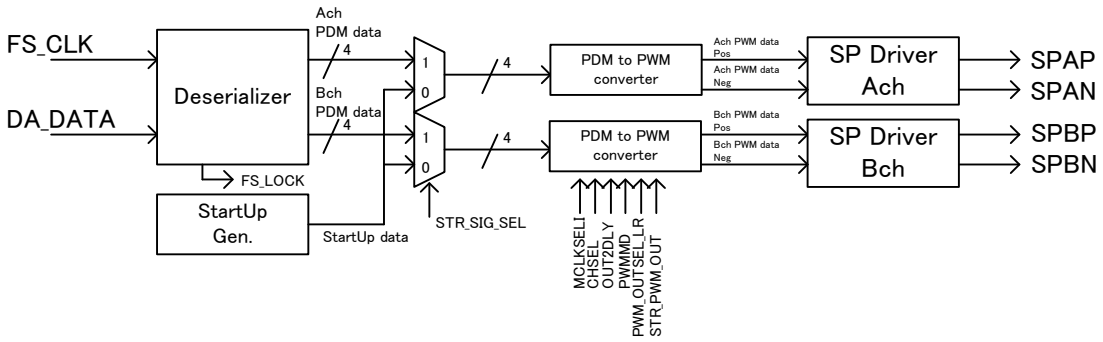
◆Audio interface specifications

CXD5247 performs signal transfer with the CXD5602 using an original format. The timing chart is shown below. The output signals to the SP can be set to the two modes of 16fs or 32fs, and the MIC output can be set to the two modes of 64fs (8Mic) or 128fs (4Mic).



Interface Timing

SP Signal Path

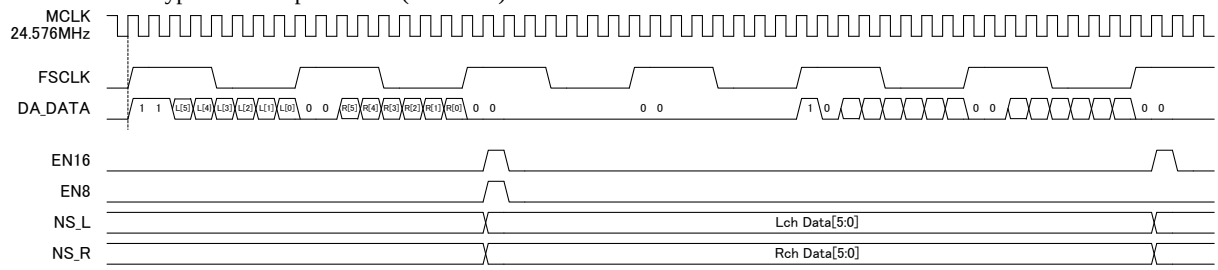


SP Signal Path

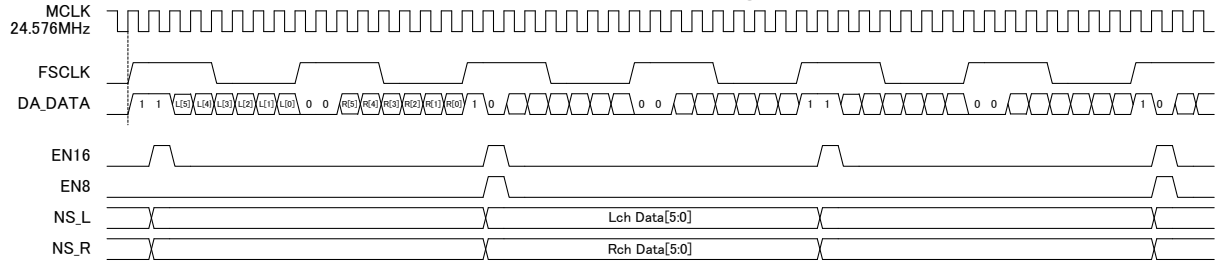
The serialized audio signals (DA_DATA, FS_CLK) output from the CXD5602 are input to the Deserialize circuit and converted into two channels of 6-bit PDM signals. These signals are converted into 1-bit PWM signals by the PDMtoPWM conversion circuit, and then output as audio signals from the drivers. In addition, a StartUP signal generation circuit is provided separately from the main line signal as a popping noise countermeasure during power-on, and when the popping noise countermeasure is set, the generated StartUp signal is selected by the register and output.

Deserialize

There are two types of the input format (16fs/32fs)..



16fs Mode Timing

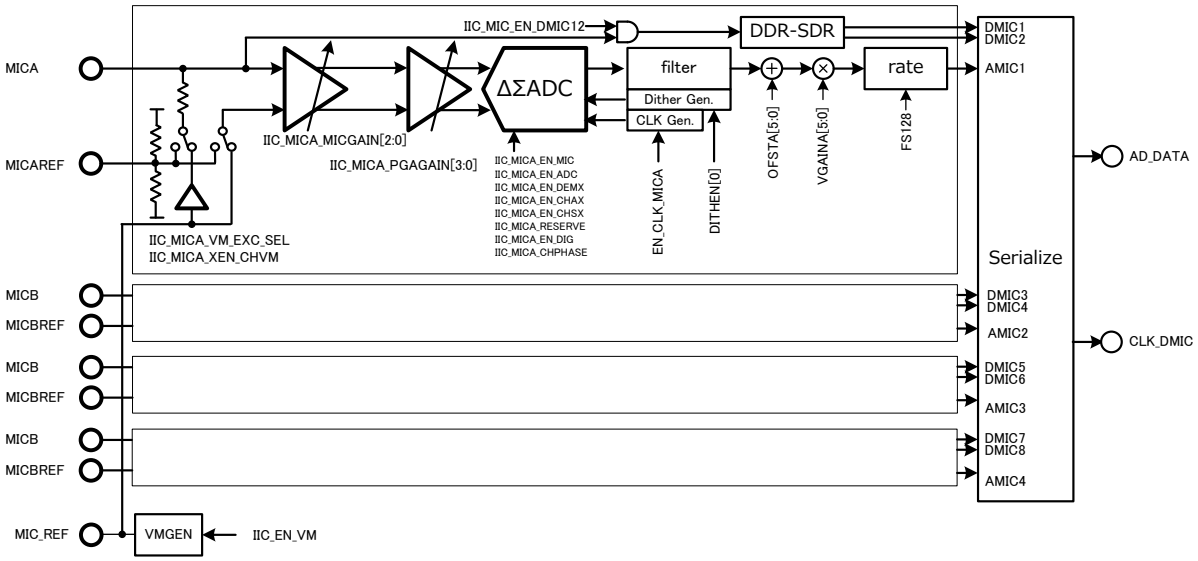


32fs Mode Timing

There are no settings for this circuit. Operation switches between 16fs and 32fs mode in accordance with the input signal.
This circuit has a function that checks for the presence of a separately input FSCLK, and the result is stored in the internal register as the FS_LOCK status information.

◆MIC signal path

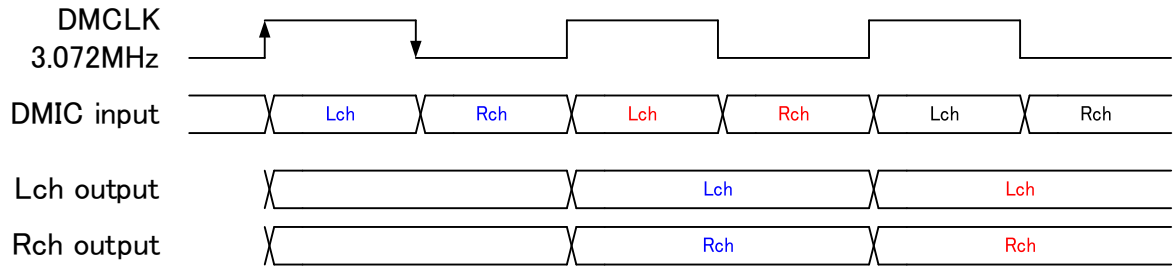
This IC has four systems of analog microphone interfaces (microphone amplifier with PGA function: ΔΣADC) and eight systems of digital microphone interfaces. The analog microphone input pins and digital microphone input pins are shared and used exclusively. The analog microphone interfaces convert the analog microphone signals to digital data. A clock generation circuit and a dither generation circuit are provided as ADC control signals. The data output by the ADC is digitally processed and converted to 1-bit PDM signals. This processing consists of a CIC-Decimator, offset adjustment circuit, gain adjustment circuit, and ΔΣModulator circuit. The output data rate can be set to 64fs or 128fs. In addition, the digital microphone interfaces perform DDR-SDR conversion on the signals. The above microphone signals (analog 4ch + digital 8ch, total 12ch) are input to the serialize circuit, converted to 8 channels or 4 channels of 1-bit serial data, and output from CXD5247 as AD_DATA.



MIC Signal Path

Digital Microphone interface

The digital microphone transfers the L/R signal at both the rising and falling edges of DMCLK (CLK for digital microphone), so this function separates the input signal into the two L and R signals. The I/O timing chart is shown below.

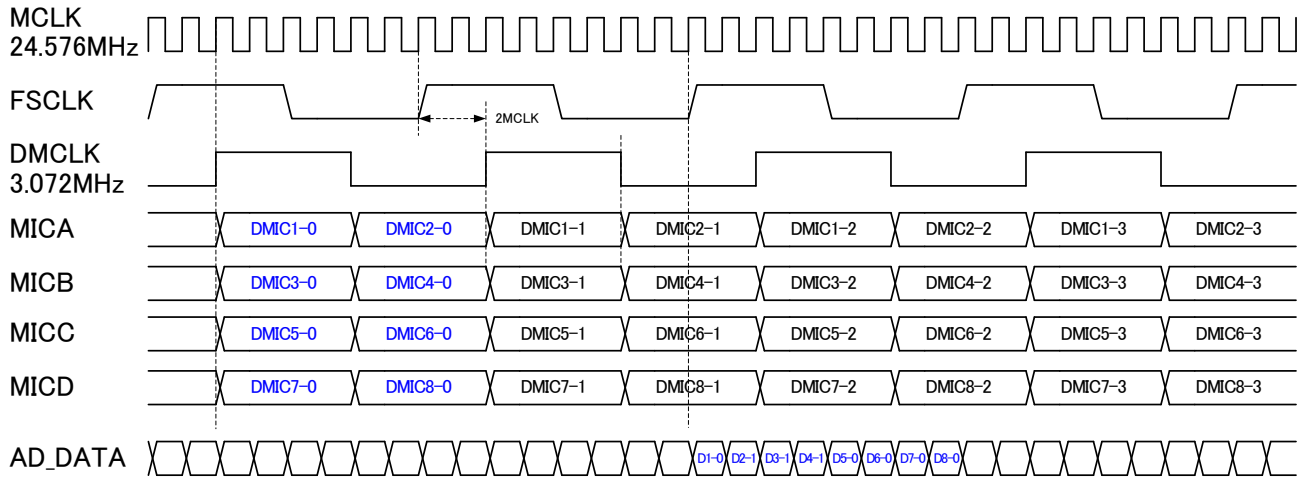


DMIC Timing

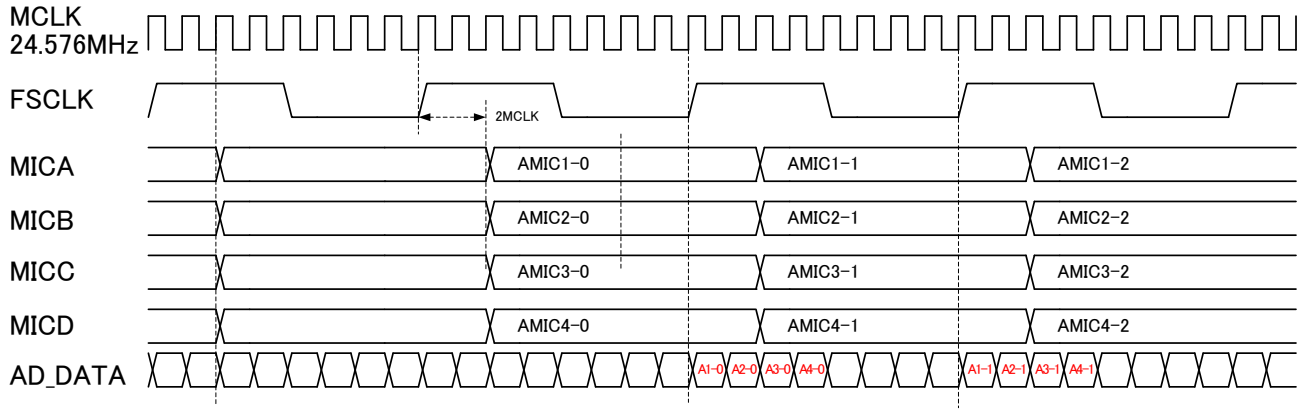
Serialize

This function selects and serializes the 4 channels of analog microphone signals and 8 channels of digital microphone signals (total 12 channels of microphone signals). The signals are output from AD_DATA of CXD5247 synchronized with FSCLK, which is the timing reference for the interface with the CXD5602. Two output formats are available: 64fs (3.072 MHz/sample) and 128fs (6.144 MHz/sample). The 64fs format enables 8-channel signal transfer, and the 128fs format enables 4-channel signal transfer. The timing chart for each format is shown below.

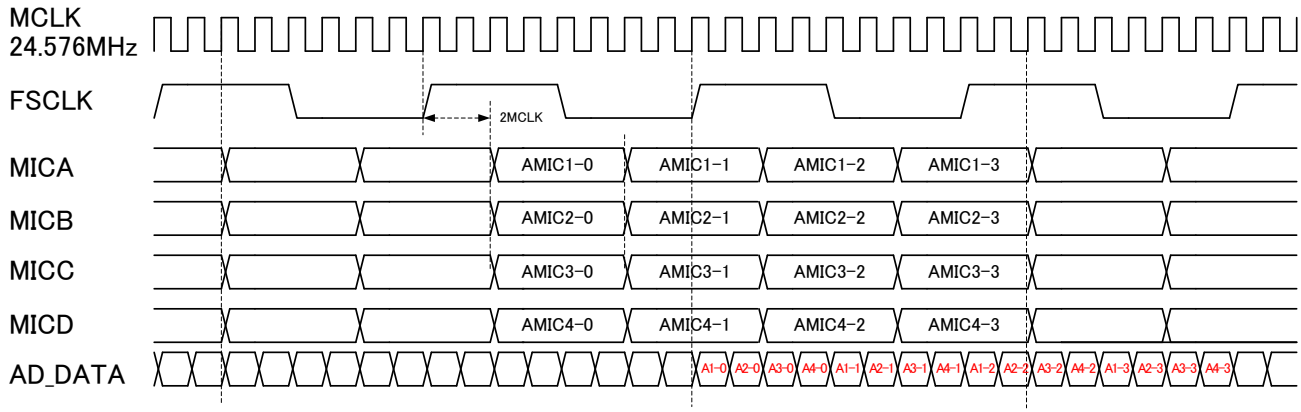
* The digital microphone signal supports only the 64fs format, and cannot be used with the 128fs format.



64fs Mode Digital MIC Interface Timing



64fs Mode Analog MIC Interface Timing

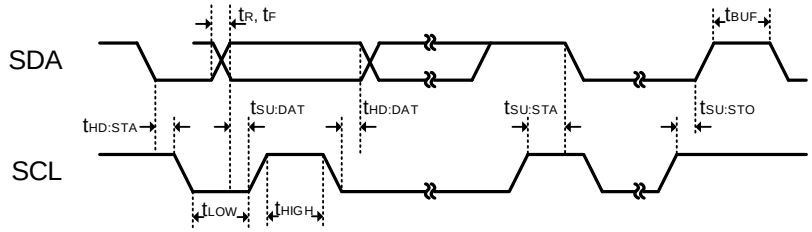


128fs Mode Analog MIC Interface Timing

Serialize mode of 64fs and 128fs is selected by SER_MODE register. Data order in AD_DATA such as D1-0, A1-0 is optionally selectable using configuration register SEL_CHx. (talble * and *)

◆I2C specifications

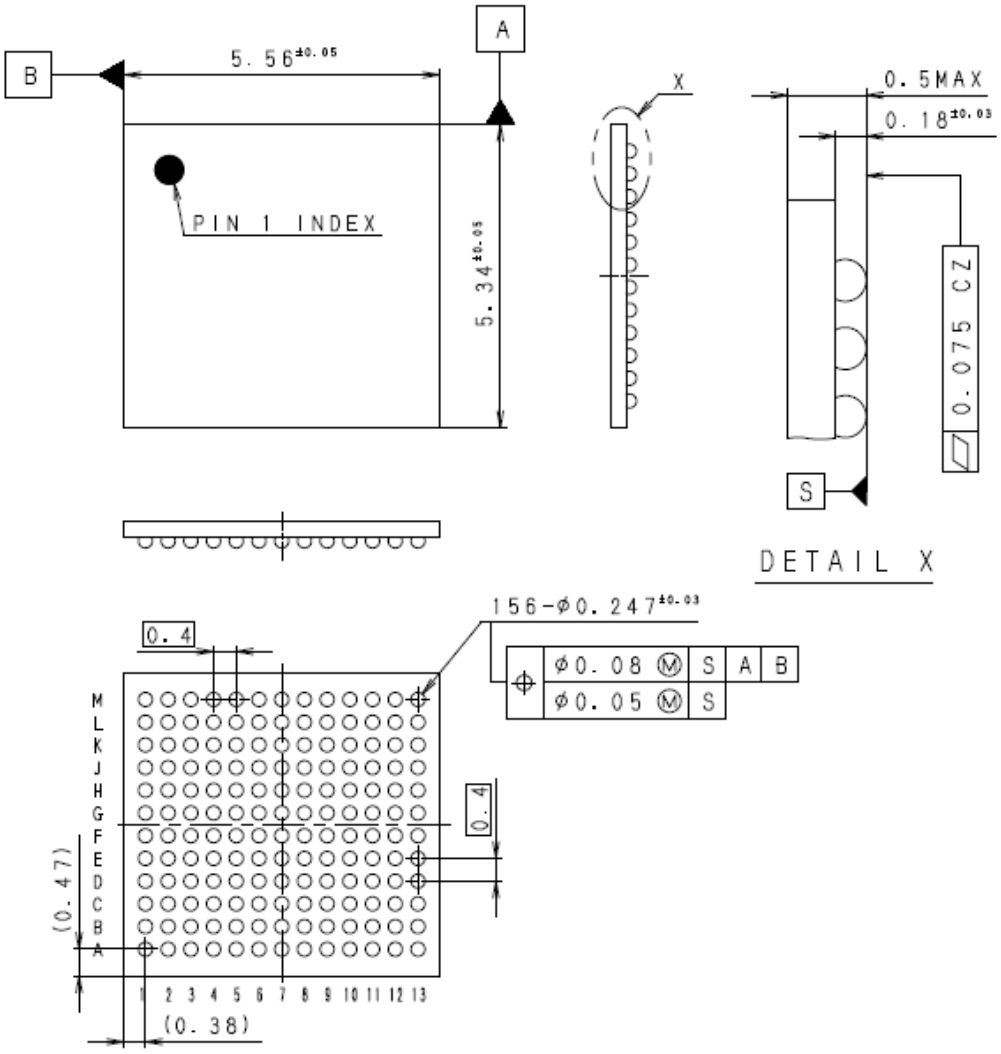
Symbol	Item	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD:STA}$	Hold time (repeat) start condition (The first clock pulse is generated after this period.)	0.6	-	us
t_{LOW}	SCL clock Low period	1.3	-	us
t_{HIGH}	SCL clock High period	0.6	-	us
$t_{SU:STA}$	Repeat start condition setup time	0.6	-	us
$t_{HD:DAT}$	Data hold time	0	-	us
$t_{SU:DAT}$	Data setup time	100	-	ns
tr	SDA signal and SCL signal rise time	-	300	ns
tf	SDA signal and SCL signal fall time	-	300	ns
$t_{SU:STO}$	Stop condition setup time	0.6	-	us
t_{BUF}	Bus free time between Stop and Start conditions	1.3	-	us
Cb	Capacitance load of each bus line	-	400	pF



Slave Address of CXD5247 Audio is 7’h1E.

Package Outline

156PIN XFBGA



PACKAGE STRUCTURE

SONY CODE	XFBGA-156S-311
JEITA CODE	S-XFBGA156-5.56x5.34-0.4
JEDEC CODE	————

PACKAGE MATERIAL	SI SUBSTRATE
TERMINAL MATERIAL	Sn-4.0Ag-0.5Cu
PACKAGE MASS	0.026g

Caution
The product of the WLCSP package should be used under light-shielded conditions.
Since the WLCSP package has a structure that a silocon wafer is exposed,
if light hits the wafer, the device may malfunction.

Notice

Purpose of Use of the Products:

Customer shall use the Products with the utmost concern for safety, and shall not use the Products for any purpose that may endanger life or physical wellbeing, or cause serious damage to property or the environment, either through normal use or malfunction.

Use of the Products for purposes other than those stipulated in this specification is strictly prohibited.

Furthermore, usage of the Products for military purposes is strictly prohibited at all times.

Safe Design:

- Customer is responsible for taking due care to ensure the product safety design of its products in which the Products are incorporated, such as by incorporating redundancy, anti-conflagration features, and features to prevent mis-operation, in order to prevent accidents resulting in injury, death, fire, or other social damage as a result of failure.

Product Information:

- The product specifications, circuit examples, and any and all other technical information and content contained in this specification, as well as any other information and materials provided to Customer in connection with the Products (collectively, "Product Information") have been provided to Customer for reference purpose only, and the availability and disclosure of such Product Information and its usage by Customer shall not be construed as giving any indication that Sony, its subsidiaries and/or its licensors will license any right, including intellectual property rights in such Product Information by any implication or otherwise.
- Furthermore, even if circuit examples are included in this specification, they are provided only for reference purpose only, and are merely examples of application. Sony, its Subsidiaries and/or their authorized representatives shall not be liable for any damage arising out of their usage.

EXCLUSION OF WARRANTY ON THE PRODUCTS:

- UNLESS OTHERWISE NOTIFIED BY US IN WRITING, OTHERWISE AGREED BETWEEN THE CUSTOMER AND SONY, ITS SUBSIDIARIES OR ANY OF THEIR AUTHORIZED REPRESENTATIVES IN WRITING, OR TO THE EXTENT PERMITTED BY LAW, THE FOLLOWING TEMS AND CONDITIONS SHALL APPLY TO THE USAGE OF THE PRODUCTS AND THE PRODUCT INFORMATION:

  THE PRODUCTS AND THE PRODUCT INFORMATION ARE PROVIDED BY SONY, ITS SUBSIDIARIES AND/OR THEIR AUTHORIZED REPRESENTATIVES "AS IS" AND WITHOUT WARRANTY OF ANY KIND AND SONY, ITS SUBSIDIARIES AND/OR THEIR AUTHORIZED REPRESENTATIVES MAKE OR HAVE MADE NO REPRESENTATION OR WARRANTY, EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE, AND EXPRESSLY DISCLAIMS ANY REPRESENTATION OR WARRANTY (I) WITH RESPECT TO ACCURACY, RELIABILITY, VALUE, UTILITY OR SAFETY OF THE PRODUCTS AND THE PRODUCT INFORMATION, OR THE ABILITY OF CUSTOMER TO MAKE USE THEREOF, (II) WITH RESPECT TO ANY IMPLEMENTATION OF THE PRODUCTS AND THE TECHNICAL INFORMATION; (III) WITH RESPECT TO MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE; OR (IV) THAT THE PRODUCTS AND THE PRODUCT INFORMATION OR ANY IMPLEMENTATION THEREOF IS OR WILL BE FREE FROM INFRINGEMENT, MISAPPROPRIATION OR VIOLATION OF ANY INTELLECTUAL PROPERTY RIGHT OR ANY OTHER RIGHT OF ANY THIRD PARTY, AND ANY EQUIVALENTS OF ANY OF THE FOREGOING UNDER THE LAWS OF ANY JURISDICTION.

  CUSTOMER HEREBY ACKNOWLEDGES AND AGREES THAT USE OF THE PRODUCTS AND THE PRODUCT INFORMATION IS AT CUSTOMER'S SOLE RISK AND THAT CUSTOMER IS RESPONSIBLE FOR THE USE OF THE PRODUCTS AND THE PRODUCT INFORMATION, INCLUDING DEFENDING ANY INFRINGEMENT CLAIM MADE AGAINST THE CUSTOMER IN RELATION WITH CUSOMTER'S USAGE OF THE PRODUCTS AND TECHNICAL INFORMATION.

  NO ORAL OR WRITTEN INFORMATION OR ADVICE GIVEN BY SONY, ITS SUBSIDIARIES OR THEIR AUTHORIZED REPRESENTATIVES SHALL CREATE A WARRANTY, DUTY OR CONDITION OR IN ANY WAY INCREASE THE SCOPE OF THIS WARRANTY.

LIMITATION OF LIABILITY:

- TO THE EXTENT PERMITTED BY LAW, SONY, ITS SUBSIDIARIES AND/OR THEIR AUTHORIZED REPRESENTATIVES SHALL NOT BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES FOR BREACH OF ANY EXPRESS OR IMPLIED WARRANTY, BREACH OF CONTRACT, NEGLIGENCE, STRICT LIABILITY OR UNDER ANY OTHER LEGAL THEORY RELATED TO THE PRODUCTS AND PRODUCT INFORMATION, INCLUDING, BUT NOT LIMITED TO, ANY DAMAGES ARISING OUT OF LOSS OF PROFITS, LOSS OF REVENUE, LOSS OF DATA, LOSS OF USE OF THE PRODUCTS OR ANY ASSOCIATED HARDWARE, DOWN TIME AND USER'S TIME, EVEN IF ANY OF THEM HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Compliance with Laws:

- Customer shall comply with all applicable laws, ordinances, rules and regulations in connection with the usage of the Products, including the export control laws or regulations of various countries and shall be fully responsible for obtaining approvals in connection with the export of the Products in accordance with such said laws, ordinances, rules and/or regulations.

Governing Law:

- This specification and the terms and conditions contained herein shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this specification and the terms and conditions contained herein shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

Notes:

- The product specifications, circuit examples, technical information and any and all other information and content relating to the Products contained in this specification may be revised or updated by Sony at Sony's sole discretion without prior notice to the Customer and Customer shall abide by their latest versions. Such revisions or updates will be made available to Customer in a way as Sony deems appropriate.
- Ensure that you have read and reviewed the notices contained in our delivery specification as well as this specification when purchasing and using the Products.