

# LM148, LM248, LM348 QUADRUPLE OPERATIONAL AMPLIFIERS

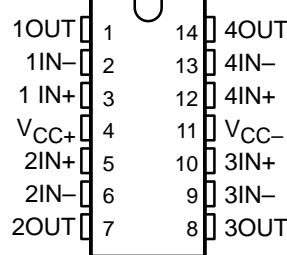
SLOS058C – OCTOBER 1979 – REVISED DECEMBER 2002

- $\mu$ A741 Operating Characteristics
- Low Supply-Current Drain . . . 0.6 mA Typ (per amplifier)
- Low Input Offset Voltage
- Low Input Offset Current
- Class AB Output Stage
- Input/Output Overload Protection
- Designed to Be Interchangeable With Industry Standard LM148, LM248, and LM348

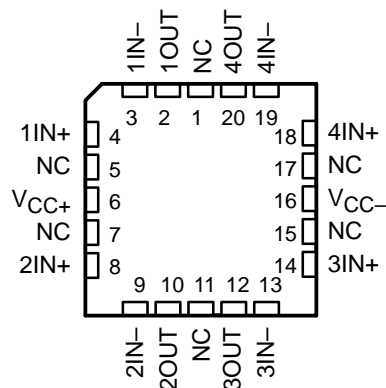
## description/ordering information

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the  $\mu$ A741. These amplifiers exhibit low supply-current drain and input bias and offset currents that are much less than those of the  $\mu$ A741.

LM148 . . . J PACKAGE  
LM248 . . . D OR N PACKAGE  
LM348 . . . D, N, OR NS PACKAGE  
(TOP VIEW)



LM148 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	$V_{IOmax}$ AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (N)	Tube of 25	LM348N	LM348N
		SOIC (D)	Tube of 50	LM348D	LM348
			Reel of 2500	LM348DR	
		SOP (NS)	Reel of 2000	LM348NSR	LM348
-25°C to 85°C	6 mV	PDIP (N)	Tube of 25	LM248N	LM248N
		SOIC (D)	Tube of 50	LM248D	LM248
			Reel of 2500	LM248DR	
		CDIP (J)	Tube of 25	LM148J	LM148J
-55°C to 125°C	5 mV	LCCC (FK)	Tube of 50	LM148FK	LM148FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# LM148, LM248, LM348 QUADRUPLE OPERATIONAL AMPLIFIERS

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## symbol (each amplifier)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ (see Note 1):	LM148	22 V
	LM248, LM348	18 V
Supply voltage, $V_{CC-}$ (see Note 1):	LM148	-22 V
	LM248, LM348	-18 V
Differential input voltage, $V_{ID}$ (see Note 2):	LM148	44 V
	LM248, LM348	36 V
Input voltage, $V_I$ (either input, see Notes 1 and 3):	LM148	-22 V
	LM248, LM348	-18 V
Duration of output short circuit (see Note 4)		Unlimited
Operating virtual junction temperature, $T_J$		150°C
Package thermal impedance, $\theta_{JA}$ (see Notes 5 and 6):	D package	86°C/W
	N package	80°C/W
	NS package	76°C/W
Package thermal impedance, $\theta_{JC}$ (see Notes 7 and 8):	FK package	5.61°C/W
	J package	15.05°C/W
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, N, or NS package		260°C
Storage temperature range, $T_{stg}$		-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at  $IN+$  with respect to  $IN-$ .
  3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
  4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
  5. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  6. The package thermal impedance is calculated in accordance with JESD 51-7.
  7. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JC}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_C)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  8. The package thermal impedance is calculated in accordance with MIL-STD-883.

## recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{CC+}$	4	18	V
Supply voltage, $V_{CC-}$	-4	-18	V



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**electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†		LM148			LM248			LM348			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 0$	25°C	1	5		1	6		1	6	mV	
		Full range		6		7.5		7.5				
$I_{IO}$ Input offset current	$V_O = 0$	25°C	4	25		4	50		4	50	nA	
		Full range		75		125		100				
$I_{IB}$ Input bias current	$V_O = 0$	25°C	30	100		30	200		30	200	nA	
		Full range		325		500		400				
$V_{ICR}$ Common-mode input voltage range		Full range	±12			±12			±12			V
$V_{OM}$ Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega$	25°C	±12 ±13			±12 ±13			±12 ±13			V
		Full range	±12			±12			±12			
		25°C	±10 ±12			±10 ±12			±10 ±12			
		Full range	±10			±10			±10			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$ , $R_L = \geq 2\text{ k}\Omega$	25°C	50	160		25	160		25	160	V/mV	
		Full range	25			15			15			
$r_i$ Input resistance‡		25°C	0.8	2.5		0.8	2.5		0.8	2.5	MΩ	
$B_1$ Unity-gain bandwidth	$A_{VD} = 1$	25°C	1			1			1			MHz
$\phi_m$ Phase margin	$A_{VD} = 1$	25°C	60°			60°			60°			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$ , $V_O = 0$	25°C	70	90		70	90		70	90	dB	
		Full range	70			70			70			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 9\text{ V to } \pm 15\text{ V}$ , $V_O = 0$	25°C	77	96		77	96		77	96	dB	
		Full range	77			77			77			
$I_{OS}$ Short-circuit output current		25°C	±25			±25			±25			mA
$I_{CC}$ Supply current (four amplifiers)	No load	$V_O = 0$				2.4 4.5			2.4 4.5			mA
		$V_O = V_{OM}$	2.4 3.6									
$V_{O1}/V_{O2}$ Crosstalk attenuation	$f = 1\text{ Hz to } 20\text{ kHz}$	25°C	120			120			120			dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for  $T_A$  is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for LM148,  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for LM248, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for LM348.

‡ This parameter is not production tested.

# LM148, LM248, LM348 QUADRUPLE OPERATIONAL AMPLIFIERS

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operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Figure 1		0.5		$\text{V}/\mu\text{s}$

## PARAMETER MEASUREMENT INFORMATION

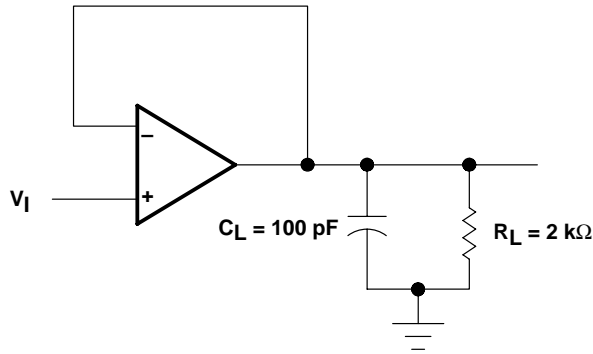


Figure 1. Unity-Gain Amplifier

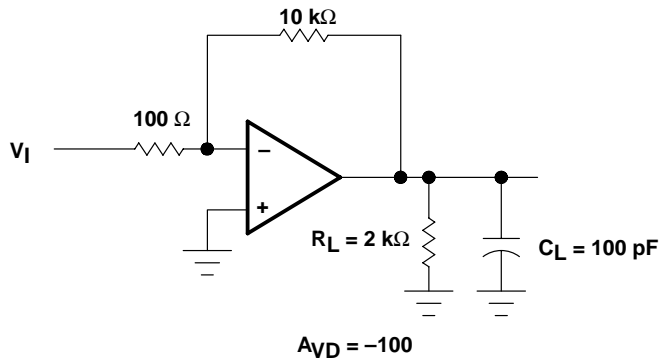


Figure 2. Inverting Amplifier

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM148 MW8	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		<a href="#">Samples</a>
LM148FKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM148FKB	<a href="#">Samples</a>
LM148J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM148J	<a href="#">Samples</a>
LM148JB	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM148JB	<a href="#">Samples</a>
LM248D	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM248	
LM248DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM248	<a href="#">Samples</a>
LM248N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM248N	<a href="#">Samples</a>
LM348D	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	
LM348DG4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	
LM348DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	<a href="#">Samples</a>
LM348DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	<a href="#">Samples</a>
LM348DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	<a href="#">Samples</a>
LM348N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM348N	<a href="#">Samples</a>
LM348NSR	LIFEBUY	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM248DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM348DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM348NSR	SO	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM248DR	SOIC	D	14	2500	356.0	356.0	35.0
LM348DR	SOIC	D	14	2500	333.2	345.9	28.6
LM348NSR	SO	NS	14	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM148FKB	FK	LCCC	20	55	506.98	12.06	2030	NA
LM248D	D	SOIC	14	50	506.6	8	3940	4.32
LM248N	N	PDIP	14	25	506	13.97	11230	4.32
LM348D	D	SOIC	14	50	506.6	8	3940	4.32
LM348D	D	SOIC	14	50	507	8	3940	4.32
LM348DG4	D	SOIC	14	50	507	8	3940	4.32
LM348DG4	D	SOIC	14	50	506.6	8	3940	4.32
LM348N	N	PDIP	14	25	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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